2581-4575
International Journal For Recent Developments in Science & Technology
Crossref
A Peer Reviewed Research Journal

Improvement of Power Quality forFuzzy Controller Based Unified Power Quality Conditioner

1Y.Hazarathaiah, 2C.Shabarinath,3S.Vivek,4G.Purushottam Naidu,5P.Rakesh,
1Assistant Professor, 2,3,4,5B-tech students Scholar
1, 2,3,4,5 Department of Electrical & Electronics Engineering,
1, 2,3,4,5G. Pullaiah College of Engineering and Technology, Nandikotkur Rd,
Near Venkayapalle, Pasupula Village, Kurnool, Andhra Pradesh 518002

Abstract:In this project Fuzzy based Unified power quality conditioner for power quality improvement is presented. Unified power quality conditioner is a compensating device which is made for mitigation of all power quality problems together. This device will reduce harmonics which affects the quality of power. Unified power quality conditioner is the combinations of series active power filter and shunt active power filter which are joined back to back by a common DC link through capacitor. The performance of the filters mainly depends on its control strategy. A Fuzzy Logic Controller (FLC) is based on fuzzy sets and fuzzy rules with their membership functions of inputs and outputs. In this paper control technique is used for series active powerfilter and shunt active power filter is synchronous Reference frame (SRF) and instantaneous PQ (IPQ) used to compensate powerquality problems by a three phase unified power quality conditioner under imbalanced and distorted load conditions. This paper accentuates improvement of power quality by using Unified power quality conditioner with proportional integral controllerandfuzzy logic controller and comparing it with & without compensating devices. The performance and behavior of the proposed controllers has been evaluated through MATLAB/SIMULINK.

Keywords-Active filter, dual control strategy, power conditioning, three-phase distribution systems, unified power qualityconditioner (UPQC), Fuzzy Logic Controller

.

I. INTRODUCTION

In recent years, many researchers give attention to solving power quality problems. These problems are appeared due to usage of reactive loads and non-linear loads. This load creates reactive power burden and harmonic problem. This harmonic pollution degrades the quality of power at transmission side as well as distribution side [1-2]. In literature, many papers have addressed these issues and have proposed the compensating devices for eliminating this problem. Usually passive filters are used to eliminate harmonics because of low cost and high efficiency.

However, this filters produce resonance with supply frequency therefore active filters are used for suppressing harmonics. The harmonics makes many undesirable effects such as increased heating losses in transformer, poor power factor, malfunction of medical equipments, and torque pulsation of motors. Power quality problems can be overcome, in real time, through the utilization of “custom power devices”(CPD) [3-4].The most commonly used CPD is unified power quality controller(UPQC), which is composed by two power converters that are connected in series and in shunt and sharing common dc voltage.A shunt converter (also known as the shunt active filter) acts as a harmonic compensator and injects the current in anti–phase with the distortion components present in the line current so that a balanced sinusoidal current flows through the feeder [5].

A series converter is responsible to compensate the major power quality problems related and with the voltage delivered to the load remain regulated and with low harmonic distortion.The required rating of series active filter is much smaller than that of a conventional shunt active filter [6]. Controllers are the most significant part of the UPQC and currently various control strategies are proposed by many researchers. Here, reference current and voltage extraction from the distorted mains is by modified synchronous reference frame technique. Fuzzy [7-8] logic control methodology has been demonstrated to allow solving uncertain and vague problems.In this paper

International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal

fuzzy logic controller is used for generation of switching pulses for PWM controllers. The advantage of using fuzzy system is simplicity, case of application, flexibility, speed and ability to deal with imprecision and uncertainties.

In order to compensate the current related problems such as load unbalance compensation, reactive power compensation , current harmonic filter shunt active power filters(APF) are used and to compensate voltage related problems such as voltage sag, voltage swell, harmonics etc series active power filters(APF) are used. Unified power quality conditioner (UPQC) [9-10] aims at integrating both shunt and series active power filters (APF) through a common dc link capacitor. Constructions wise both unified power quality conditioner (UPQC) and unified power flow controller (UPFC) both are similar. Unified power quality conditioner (UPQC) aims at [11-12] conditioning the power supply by eliminating the disturbances that adversely affect the performance of the load in power system. Unified power quality conditioner (UPQC) is used to improve the quality of power on power distribution system at the point of installation.
The FC is based on linguistic variable set theory and does not require a mathematical model. Generally, the input variables are error and rate of change of error. If the error is coarse, the FC provides coarse tuning to the output variable and if the error is fine, it provides fine tuning to the output variable [13].

In the normal operation of UPQC, the control circuitry of shunt APF calculates the compensating current for the current harmonics and the reactive power compensation. In the conventional methods, the DC link capacitor voltage [14] is sensed and is compared with a reference value. The error signal thus derived is processed in a controller.

II. UPQC TOPOLOGY DESCRIPTION

The UPQC topology employed to implement the dual compensation strategy presented in this paper is shown in Fig.1.It comprises both three-leg (3-Leg) and four-leg (4-Leg) PWM converters sharing the same dc-link.

The UPQC is connected between a 3P3W power supply distribution system and a 3P4W plant site composed of several types of three-phase and single-phase loads. It is assumed that the single-phase loads use the neutral conductor to operate. In this case, a 3P4W distribution system is necessary, which is composed of three power conductors and a neutral conductor to feed the loads. Thus, as can be noted in the UPQC-based 3P4 Distribution system shown in Fig.1, the neutral current flows through the wire conductor connected to the fourth leg of the shunt 4-Leg PWM converter.

The 4-Leg PWM converter was chosen to act as the shunt APF, because it is able to operate with lower DC-link voltage amplitude when compared to the 3-Leg PWM split-capacitor topology. In addition, the 3-Leg split capacitor topology requires an additional control loop to compensate its inherent dc-link capacitor voltage unbalances. Although the 4-Leg converter has a greater number of switches, the power rating of the devices that compose its fourth leg is reduced, because the current that flows through the neutral conductor in most cases is low.

a) Dual Compensation Principle

In order to make the input currents sinusoidal, balanced and in phase with the utility voltages, in the dual compensating strategy, the series PWM converter is controlled to operate as a sinusoidal current source. In this case, its impedance must be high enough to isolate the harmonic currents generated by the nonlinear loads. On the other hand, the parallel PWM converter also makes the output voltages sinusoidal, balanced, regulated and in phase with the utility voltages. In other words, it is controlled to operate as a sinusoidal voltage source, such that its impedance must be sufficiently low to absorb the load harmonic currents.

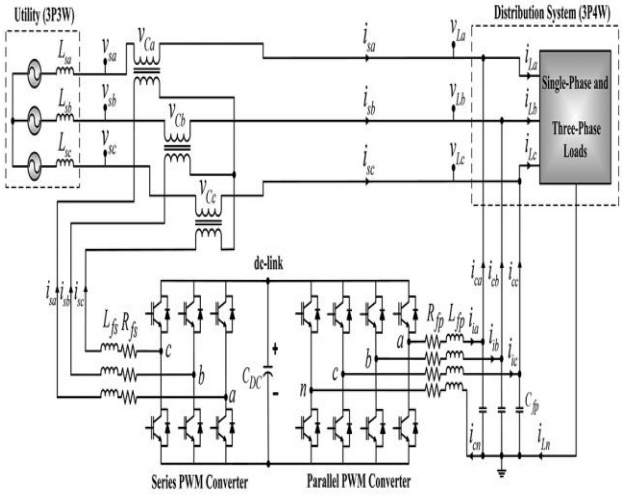


Fig.1. 3P4W distribution system based on UPQC topology connected to 3P3W power system

International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal

Since the series and parallel converters have high and low impedances, respectively, the load harmonic currents flow naturally through the parallel converter. Furthermore, compensation for load unbalances is ensured by controlling the series converter to follow sinusoidal and balanced references so that the negative and zero sequence components are compensated. Finally, the fundamental reactive power compensation is ensured by controlling the series converter current references to be in phase with the utility voltages.

On the other hand, the utility harmonic voltages and unbalances are compensated ensuring that the controlled output voltages follow sinusoidal and balanced references such that the amplitude differences between the input and output voltages will appear across the series coupling transformers, meaning that any utility voltage disturbances are naturally compensated. This makes the dual compensating strategy more attractive than the conventional strategy, considering that the load is less affected by the occurrence of grid voltage disturbances, such as voltage sags. This is possible because, different from the conventional strategy in which the series converter controls the output voltages, in the dual compensating strategy this task is entirely assumed by the parallel converter.

III. MODELING OF SERIES AND PARALLEL CONVERTERS

The modeling of the series and parallel PWM converters are presented in this section. In addition, the voltage and current controllers implemented in the SRF (dq0 axes) are discussed.

a) Series Converter Modeling

The state-space system and the transfer functions of the series converter in the dq axes are obtained based on a mathematical model. The modeling is accomplished considering that all involved inductances and resistances are identical, as follows: $L_{fsa} = L_{fsa} = L_{fsa} = L_{fsb} = L_{fsc} = L_{fs}$ and $R_{fsa} = R_{fsb} = R_{fsc} = R_{fs}$. By means of Fig.1, the equations that represent the system are given by (1) and (2)

$$u_{sab\_PWM} = v_{L_{fsa}} + v_{R_{fsa}} + v_{C_{ab}} - v_{R_{fsb}} - v_{L_{fsb}} \quad (1)$$

$$u_{sbc\_PWM} = v_{L_{fsb}} + v_{R_{fsb}} + v_{C_{bc}} - v_{R_{fsc}} - v_{L_{fsc}} \quad (2)$$

Where u_{sab} PWM and u_{sbc} PWM are the respective PWM voltages at the 3-Leg series converter terminals considering the voltages of the PWM series converter in thedq axes (usd_PWM and u_{sq}_PWM), the state-space equation is given by

$$\dot{x}_{\mathrm{sdq}}(t) = A_{\mathrm{sdq}} x_{\mathrm{sdq}}(t) + B_{\mathrm{sdq}} u_{\mathrm{sdq}}(t) + F_{\mathrm{sdq}} w_{\mathrm{sdq}}(t) \quad (3)$$

Where

$$\dot{x}_{\mathrm{sdq}}(t) = \begin{bmatrix} \frac{di_{\mathrm{sd}}}{dt} \\ \frac{di_{\mathrm{sq}}}{dt} \end{bmatrix}, \; x_{\mathrm{sdq}}(t) = \begin{bmatrix} i_{\mathrm{sd}} \\ i_{\mathrm{sq}} \end{bmatrix}, \; u_{\mathrm{sdq}} = \begin{bmatrix} u_{sd\_\mathrm{PWM}} \\ u_{sq\_\mathrm{PWM}} \end{bmatrix}$$

$$w_{\mathrm{sdq}}(t) = \begin{bmatrix} v_{\mathrm{cd}} \\ v_{\mathrm{cq}} \end{bmatrix}, \; A_{\mathrm{sdq}} = \begin{bmatrix} -\frac{R_{fs}}{L_{fs}} & \omega \\ -\omega & -\frac{R_{fs}}{L_{fs}} \end{bmatrix}$$

$$B_{\mathrm{sdq}} = \frac{1}{3L_{fs}} \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

$$F_{\mathrm{sdq}} = \frac{1}{3L_{fs}} \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix}.$$

Thereby, based on (3), the series converter average model represented as a signal flow graph is shown in the dotted area of Fig.2 (a). In addition, the current controller into the *dq*axes is also shown, where *Gs*(PI)*d* and *Gs*(PI)*q* represent the transfer functions of the PI current controllers; D_{sd} and D_{sq} arethe duty cycles; V_{dc} is the dc-bus voltage; and *K*PWM is thegain of the PWM modulator given by *K*PWM = 1/*P*PWM [31],where*P*PWM is the peak value of the PWM triangular carrier implemented in the digital signal processor (DSP). The current coupling between the *dq*axes, shown in the average model of Fig.2 (a), is eliminated by using the scheme presented inFig. 2(b), where the dotted blocks represent the decoupling effects implemented in the block diagram shown in Fig. 2(a).

Thus, based on Fig.2 (a), the transfer functions of the closed loop system can be represented by (4), where $Kp_{s(d,q)}$and$Ki_{s(d,q)}$ are the proportional and integral controller gains, and$i^{*}_{s(d,q)}$ represents the continuous current references in the *dq*coordinates

$$\frac{i_{S(d,q)}(s)}{i^{*}_{S(d,q)}(s)} = \frac{X_1\left(Kp_{s(d,q)}s + Ki_{s(d,q)}\right)}{L_{fs}s^2 + \left(R_{fs} + X_1 Kp_{s(d,q)}\right)s + X_1 Ki_{s(d,q)}} \quad (4)$$

Where X1 = $K_{PWM}V_{dc}$

b) Parallel Converter Modeling

The state-space system and the transfer functions of the parallel converter in the dq0 axes are obtained based on a mathematical model. The modeling is accomplished considering that all involved inductances, resistances and capacitances are identical, as follows: $L_{fpa} = L_{fpb} = L_{fpc} = L_{fpn} = L_{fp}$, $R_{fpa} = R_{fpb} = R_{fpc} = R_{fpn} = R_{fp}$, and $C_{fpa} = C_{fpb} = C_{fpc} = C_{fp}$.

By means of Fig.1, the equations that represent the system are given by (5), (6), and (7) as follows:

International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal

$$u_{\text{pan\_PWM}} = R_{\text{fpa}} \cdot i_{\text{ia}} + L_{\text{fpa}} \frac{di_{\text{ia}}}{dt} + v_{\text{La}} + L_{\text{fpn}} \frac{di_{\text{cn}}}{dt} + R_{\text{fpn}} \cdot i_{\text{cn}} \quad (5)$$

$$u_{\text{pbn\_PWM}} = R_{\text{fpb}} \cdot i_{\text{ib}} + L_{\text{fpb}} \frac{di_{\text{ib}}}{dt} + v_{\text{Lb}} + L_{\text{fpn}} \frac{di_{\text{cn}}}{dt} + R_{\text{fpn}} \cdot i_{\text{cn}} \quad (6)$$

$$u_{\text{pcn\_PWM}} = R_{\text{fpc}} i_{\text{ic}} + L_{fcc} \frac{di_{\text{ic}}}{dt} + v_{\text{Lc}} + L_{\text{fpn}} \frac{di_{\text{cn}}}{dt} + R_{\text{fpn}} \cdot i_{\text{cn}} \quad (7)$$

Where$u_{\text{pan_}}$PWM, $u_{\text{pbn_}}$PWM, and $u_{\text{pcn_}}$PWM are the respectivePWM voltages at the terminals *a*, *b*, and *c* of the 4-Leg parallel converter.

The capacitor currents of the output filters ($i_{\text{Cfpa, iCfp b}}$ $\text{hand}_{\text{icap c)}}$ are given by

$$i_{C_{\text{fpa}}} = C_{\text{fpa}} \frac{dv_{\text{La}}}{dt} = i_{\text{ia}} - i_{\text{ca}} \quad (8)$$

$$i_{C_{\text{fpb}}} = C_{\text{fpb}} \frac{dv_{\text{Lb}}}{dt} = i_{\text{ib}} - i_{\text{cb}} \quad (9)$$

$$i_{C_{\text{fpc}}} = C_{\text{fpc}} \frac{dv_{\text{Lc}}}{dt} = i_{\text{ic}} - i_{\text{cc}} \quad (10)$$

Wherei_{ia}, i_{ib}, and i_{ic} are the currents of the inductors, and ica,icb, and icc are the output currents of the parallel converter.

Considering the PWM converter voltages of the parallel synchronous rotating frame the state-space equation is found as

$$(u_{\text{pd\_PWM}}, u_{\text{pq\_PWM}}, \text{and } u_{\text{p0\_PWM}}),$$

$$\dot{x}_{\text{pdq0}}(t) = A_{\text{pdq0}} x_{\text{pdq0}}(t) + B_{\text{pdq0}} u_{\text{pdq0}}(t) + F_{\text{pdq0}} w_{\text{pdq0}}(t) \quad (11)$$

Where

$$\dot{x}_{\text{pdq0}}(t) = \left[\frac{di_{\text{id}}}{dt} \; \frac{di_{\text{iq}}}{dt} \; \frac{di_{\text{i0}}}{dt} \; \frac{dv_{\text{Ld}}}{dt} \; \frac{dv_{\text{Lq}}}{dt} \; \frac{dv_{\text{L0}}}{dt} \right]^T$$

$$x_{\text{pdq0}}(t) = \left[i_{\text{id}} \; i_{\text{iq}} \; i_{\text{i0}} \; v_{\text{Ld}} \; v_{\text{Lq}} \; v_{\text{L0}} \right]^T$$

$$u_{\text{pdq0}} \begin{bmatrix} u_{\text{pd\_PWM}} \\ u_{\text{pq\_PWM}} \\ u_{\text{p0\_PWM}} \end{bmatrix}, \; w_{\text{pdq0}} \begin{bmatrix} i_{C_{\text{fpd}}} \\ i_{C_{\text{fpq}}} \\ i_{C_{\text{fp0}}} \end{bmatrix}$$

$$A_{\text{pdq0}} = \begin{bmatrix} -\frac{R_{\text{fp}}}{L_{\text{fp}}} & \omega & 0 & -\frac{1}{L_{\text{fp}}} & 0 & 0 \\ -\omega & -\frac{R_{\text{fp}}}{L_{\text{fp}}} & 0 & 0 & -\frac{1}{L_{\text{fp}}} & 0 \\ 0 & 0 & -\frac{R_{\text{fp}}}{L_{\text{fp}}} & 0 & 0 & -\frac{1}{4L_{\text{fp}}} \\ \frac{1}{C_{\text{fp}}} & 0 & 0 & 0 & \omega & 0 \\ 0 & \frac{1}{C_{\text{fp}}} & 0 & -\omega & 0 & 0 \\ 0 & 0 & \frac{1}{C_{\text{fp}}} & 0 & 0 & 0 \end{bmatrix}$$

$$B_{\text{pdq0}} = \begin{bmatrix} \frac{1}{L_{\text{fp}}} & 0 & 0 \\ 0 & \frac{1}{L_{\text{fp}}} & 0 \\ 0 & 0 & \frac{1}{4L_{\text{fp}}} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

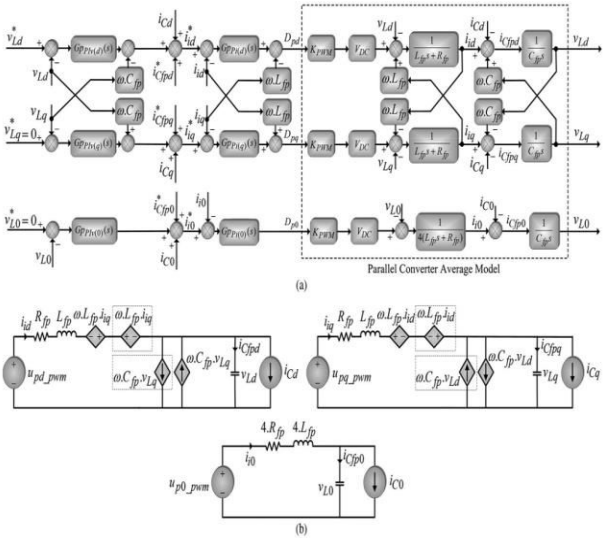


Fig.2. Parallel converter: (a) signal flow graph of the voltage controllers and average model; (b) model of the uncoupled system in SRF dq0 axes.

$$F_{\text{pdq0}} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ -\frac{1}{C_{\text{fp}}} & 0 & 0 \\ 0 & -\frac{1}{C_{\text{fp}}} & 0 \\ 0 & 0 & -\frac{1}{C_{\text{fp}}} \end{bmatrix}$$

Thereby, based on (11), the parallel converter average model represented as a signal flow graph is shown in the dotted area ofFig.3 (a). In addition, the voltage and current controllers into the*dq*0 axes are presented.

Where*Gp*PI*v* (*d*), *Gp*PI*v* (*q*), and *p*PI*v* (0) represent the transfer functions of the PI voltage controllers (outer loops); *Gp*Pi (*d*), *Gp*Pi (*q*), and *Gp*Pi (0) are the transfer functions of the proportional current

International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal

controllers (inner loops); and *D*pd, *D*pq, and *D*p0 are the duty cycles. The current and voltage coupling between the *dq*axes shown in the averagemodel of Fig.3 (a) is eliminated by using the scheme presented in Fig.3 (b), where the dotted blocks represent the decoupling effects, which are implemented in the block diagram shown in Fig.3 (a).

Thus, based on Fig.3(a), the transfer functions of the closed-loop system can be represented by (3.12) and (13), where*Kpp*(*d,q*), *Kip*(*d,q*), and *Kip*(0) are the proportional and integral gains of the controllers (outer voltage control loop), *Kp*PI(*d,q*)and *Kp*PI(0) are the proportional gains (inner current-control loop), and $v^*_{L(d,q,0)}(s)$ represents the continuousvoltage references in the dq0 coordinates.

The currents of the filter capacitors icfp(d,q,0) shown in Fig.3(a) are estimated considering the derivatives of the measured output voltages (vLa,b,c)and the respective capacitances(Cfpa,b,c)

$$\frac{v_{L(d,q)}(s)}{v^*_{L(d,q)}(s)} = \frac{X_{1(d,q)}s^2 + X_{2(d,q)}s + X_{3(d,q)}}{Y_{1(d,q)}s^3 + Y_{2(d,q)}s^2 + Y_{3(d,q)}s + Y_{4(d,q)}} \quad (12)$$

$$\frac{v_{L(0)}(s)}{v^*_{L(0)}(s)} = \frac{X_{1(0)}s^2 + X_{2(0)}s + X_{3(0)}}{Y_{1(0)}s^3 + Y_{2(0)}s^2 + Y_{3(0)}s + Y_{4(0)}} \quad (13)$$

IV. STABILITY ANALYSIS OF THE SYSTEM

The stability study of the UPQC system, which involves the series and parallel converters. The aim of this study was to verify the ability of the system to remain stable even under load disturbances.

a) Series APF

Considering the signal flow graph of the current controller and the series converter average model shown in Fig.2 (a), the closed-loop transfer function in the d-q coordinates can be represented by (4). Thereby, the stability analysis of the series converter involves only the second-order denominator (λi) of (4). By applying the Routh–Hurwitz stability criterion, the necessary and sufficient condition for ensuring the series converter stability is that all the coefficients of λi must have the same sign. As can be noted, all the coefficients are positive, meaning that the series converter control is always stable. In addition, load transients only affect the generation of the series current references. Therefore, since the reference currents are always sinusoidal, it is possible to assume that the series converter remains acting as a sinusoidal current source even when load transients occur.

b)Parallel APF

Considering the signal flow graph of the voltage controllers and the parallel converter average model shown in Fig.3 (a), the closed-loop transfer functions in the dq0 coordinates can be represented by (12) and (13). Considering that the PI controller gains KpPI = KpPI(d,q) = KpPI(0)/4,Kpp = Kpp(d,q) = Kpp(0), and Kip = Kip(d,q) = Kip(0),the same transfer function is obtained for each control loop implemented in the d, q, and 0 coordinates as given by (14), allowing the study of the voltage control loops by means of a unique transfer function Gv (s). In addition, it is assumed that the individual control loops in the dq0 coordinates are obtained taking into account the coupling effects between the d-q coordinates shown in Fig.3.

$$G_v(s) = \frac{v_{L(d,q,0)}(s)}{v^*_{L(d,q,0)}(s)} = \frac{(1+K)\left[X_{1(d,q,0)}s^2 + X_{2(d,q,0)}s + X_{3(d,q,0)}\right]}{Y_{1(d,q,0)}s^3 + Y_{2(d,q,0)}s^2 + Y_{3(d,q,0)}s + Y_{4(d,q,0)}} \quad (14)$$

Where

$$X_{1(d,q,0)} = K_{\mathrm{PWM}}V_{\mathrm{dc}}C_{\mathrm{fp}}Kp_{\mathrm{PI}}$$
$$X_{2(d,q,0)} = K_{\mathrm{PWM}}V_{\mathrm{dc}}Kp_{\mathrm{PI}}Kp_p$$
$$X_{3(d,q,0)} = Y_{4(d,q,0)} = K_{\mathrm{PWM}}V_{\mathrm{dc}}Kp_{\mathrm{PI}}Ki_p$$
$$Y_{1(d,q,0)} = C_{\mathrm{fp}}L_{\mathrm{fp}}$$
$$Y_{2(d,q,0)} = C_{\mathrm{fp}}(K_{\mathrm{PWM}}V_{\mathrm{dc}}Kp_{\mathrm{PI}} + R_{\mathrm{fp}})$$
$$Y_{3(d,q,0)} = K_{\mathrm{PWM}}V_{\mathrm{dc}}Kp_{\mathrm{PI}}Kp_p + 1.$$

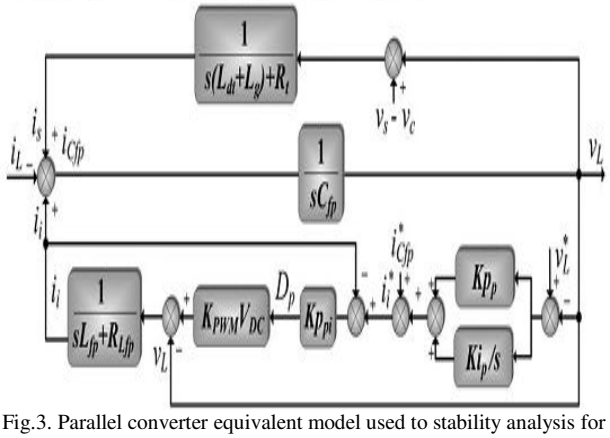


Fig.3. Parallel converter equivalent model used to stability analysis for thedq0 voltage control loops

International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal

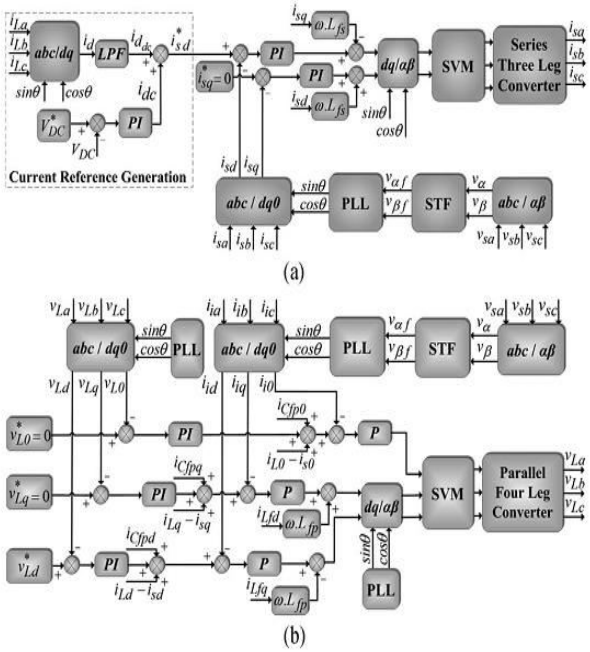


Fig.4. Signal flow graphs of the reference generation and control scheme of both series and parallel PWM converters: (a) reference current generation and the input current controllers; (b) output voltage controllers.

However, it is not possible to analyze how the load current transients will interfere in the controls of the UPQC output voltages only by using the transfer function Gv (s). Thus, Fig.4presents the block diagram, which is based on the control loops shown in Fig.3 (a), as well as the aforementioned considerations. Thus, the load current (iL) is considered as an input of the system, whereas the voltage (vL) is the output. In addition, in order to obtain an adequate representation of the system, the source current (is) is calculated from both the output voltage(vL) and input voltage (vs), taking into account the leakage inductances and resistances of the series coupling transformers (Ldt and Rt), as well as the grid equivalent inductances(Lg). Thereby, from Fig. 3.4, the closed-loop transfer functionGiv(s) = vL (d, q, 0) (s) /iL (d, q, 0) (s) can be obtained by (15).By applying the Routh–Hurwitz stability criterion, two conditions must be met: 1) all the polynomial coefficients of the denominator must have the same sign and 2) the inequalityY2Y3 > Y1Y4 must be respected. Therefore, by inspecting the denominator of (15), the first condition is always met. On the other hand, the second condition can be met by adjusting the PIcontroller gains. Thus, taking into account the aforementioned conditions, the system will always be stable, even when load transients occur

$$G_{vi}(s) = \frac{v_{L(d,q,0)}(s)}{i_{L(d,q,0)}(s)} = \frac{X_1 s^2 + X_2 s + X_3}{Y_1 s^3 + Y_2 s^2 + Y_3 s + Y_4} \quad (15)$$

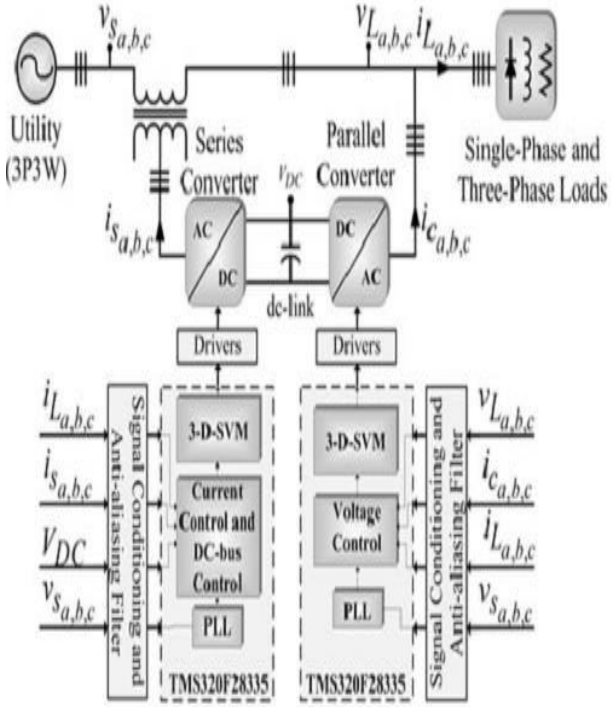


Fig.5. UPQC implementation

V. CONTROL REFERENCES OF THE SERIES AND PARALLEL CONVERTERS

The strategies used to generate the sinusoidal reference quantities used to control the series and the parallel converters are presented. As aforementioned, both the current and voltage control references are controlled to be in phase with the utility voltages. Since the controlled voltages and currents are sinusoidal quantities, a significant advantage is attained when the dual compensating strategy is compared with the conventional strategy, whose controlled quantities are always non-sinusoidal. This advantage is highlighted mainly because the control references into the SRF-based controllers are continuous, leading to reduced errors in the steady state of the PIcontrollers.

a) Series Converter Reference Currents

The current-control loop of the series converter is shown in the signal flow graph of Fig.5 (a). The continuous reference current in the SRF direct axis d is defined byi_{sd}^{*}, which is able to make the serial converter synthesize the sinusoidal input currents (isa, isb, isc). As can be noted, the three-dimensional space vector

International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal

modulation (3-D-SVM) technique is used in the series converter.

The reference currenti_{sd}^{*} is obtained by measuring the load currents (iLa, iLb, iLc) and converting them to the rotating reference frame. Thus, the direct current (id) is achieved by means of (16) and (17), whereas the utility phase-angle θ used to calculate the coordinates of the unit vectors sin θ and cos θ,is obtained from the three-phase PLL system. Next, a low-pass filter (LPF) is employed to obtain the direct component (id_{dc}), which represents, in the SRF, the active portions of the load currents (i_{La}, i_{Lb}, i_{Lc}). In other words, id_{dc} represents the positive sequence components of the load currents

$$\begin{bmatrix} i_\alpha \\ i_\beta \\ i_0 \end{bmatrix} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \begin{bmatrix} i_{\mathrm{La}} \\ i_{\mathrm{Lb}} \\ i_{\mathrm{Lc}} \end{bmatrix} \quad (16)$$

$$i_d = i_\alpha \cos\theta + i_\beta \sin\theta \quad (17)$$

The control of the power balance flow through the UPQC must be taking into account in order to maintain the dc-bus voltage constant. Thereby, the final reference currenti_{sd}^{*} is calculated byusing (18), where i_{dc} is added to i_{ddc}. Thus, i_{dc} represents the control action of the dc-bus voltage controller that compensates the inherent losses of the filter elements and semiconductor devices. In addition, i_{dc} controls the balance of the power flow through the UPQC when different amplitudes between the input voltages (v_{sa}, v_{sb}, v_{sc}) and output voltages (v_{La}, v_{Lb}, v_{Lc}) occur.

$$i_{\mathrm{sd}}^{*} = i_{\mathrm{dc}} + i_{d_{\mathrm{dc}}} \quad (18)$$

The reference current of the quadrature axisi_{sq}^{*} and i_{s0}^{*} areset to zero since the series converter synthesizes only positive sequence components (active currents), such that sinusoidal and balanced currents are achieved.

b) Parallel Converter Reference Voltages

The voltage control loop of the parallel converter is shown in the signal flow graph of Fig.5 (b). The reference voltage in theSRF direct axis d is defined byv_{Ld}^{*}. Its constant and continuousvalue represents the ac voltages (vLa, vLb, vLc) provided to theload. The reference voltages of the quadrature axis q v_{Lq}^{*}andv_{L0}^{*} are set to zero since sinusoidal and balanced voltages aredesirable. As can be noted, the 3-D-SVM technique is employed in the parallel converter.

VI. FUZZY LOGIC CONTROLLER

The Fuzzy control is a methodology to represent and implement a (smart) human's knowledge about how to control a system. A fuzzy controller is shown in Figure.6. The fuzzy controller has several components:

- A rule base that determines on how to perform control
- Fuzzification that transforms the numeric inputs so that the inference mechanisms can understand.
- The inference mechanism uses information about the current inputs and decides the rules that are suitable in the current situation and can form conclusion about system input.
- Defuzzification is opposite of Fuzzification which converts the conclusions reached by inference mechanism into numeric input for the plant.

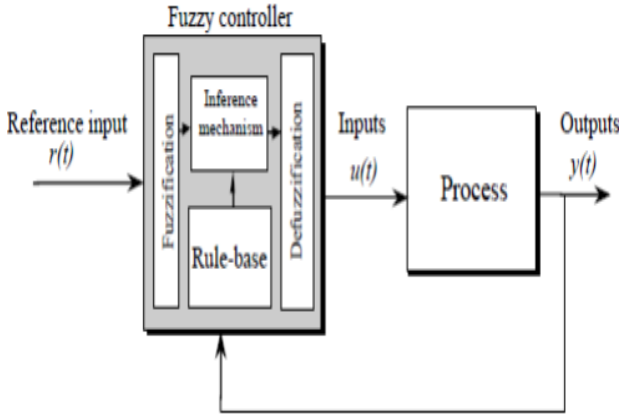


Fig.6 Fuzzy Control System

Fuzzy logic is a form of logic that is the extension of Boolean logic, which incorporates partial values of truth. Instead of sentences being "completely true" or "completely false," they are assigned a value that represents their degree of truth. In fuzzy systems, values are indicated by a number (called a truth value) in the range from 0 to 1, where 0.0 represents absolute false and 1.0 represents absolute truth. Fuzzification is the generalization of any theory from discrete to continuous. Fuzzy logic is important to artificial intelligence because they allow computers to answer 'to a certain degree' as opposed to in one extreme or the other. In this sense, computers are allowed to think more 'human-like' since almost nothing in our perception is extreme, but is true only to a certain degree.

Table 1: IF-THEN rules for fuzzy inference system

International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal

u(t)		e(t)						
		NB	**NM**	**NS**	**ZO**	**PS**	**PM**	**PB**
Δe(t)	**NB**	NB	NB	NB	NB	NM	NS	ZO
	NM	NB	NB	NB	NM	NS	ZO	PS
	NS	NB	NB	NM	NS	NS	PS	PS
	ZO	NB	NM	NS	ZO	ZO	PM	PM
	PS	NM	NS	ZO	PS	PS	PB	PB
	PM	NS	ZO	PS	PM	PM	PB	PB
	PB	ZO	PS	PM	PB	PB	PB	PB

The fuzzy rule base can be read as follows
IF e(t) is NB and Δe(t) is NB **THEN** u(t) is NB **IF** e(t) is <negative big> and Δe(t) is <negative big>**THEN** u(t) is <negative big>.

VII. MATLAB/SIMULINK RESULTS

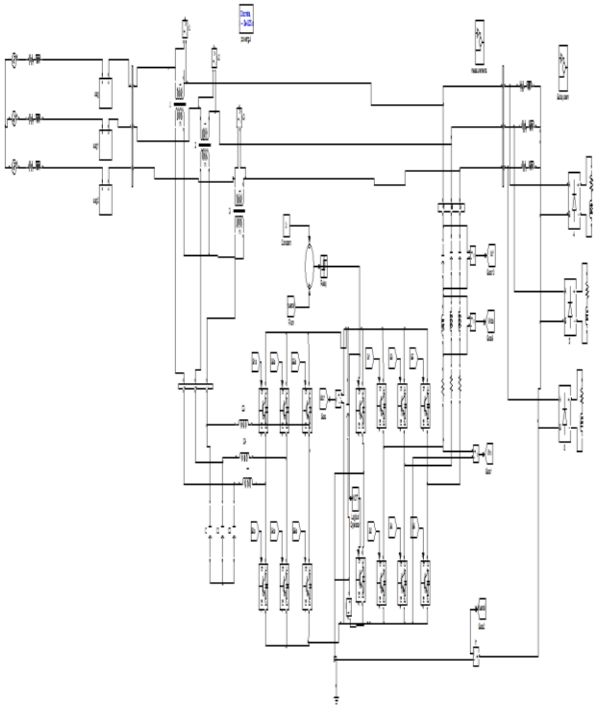
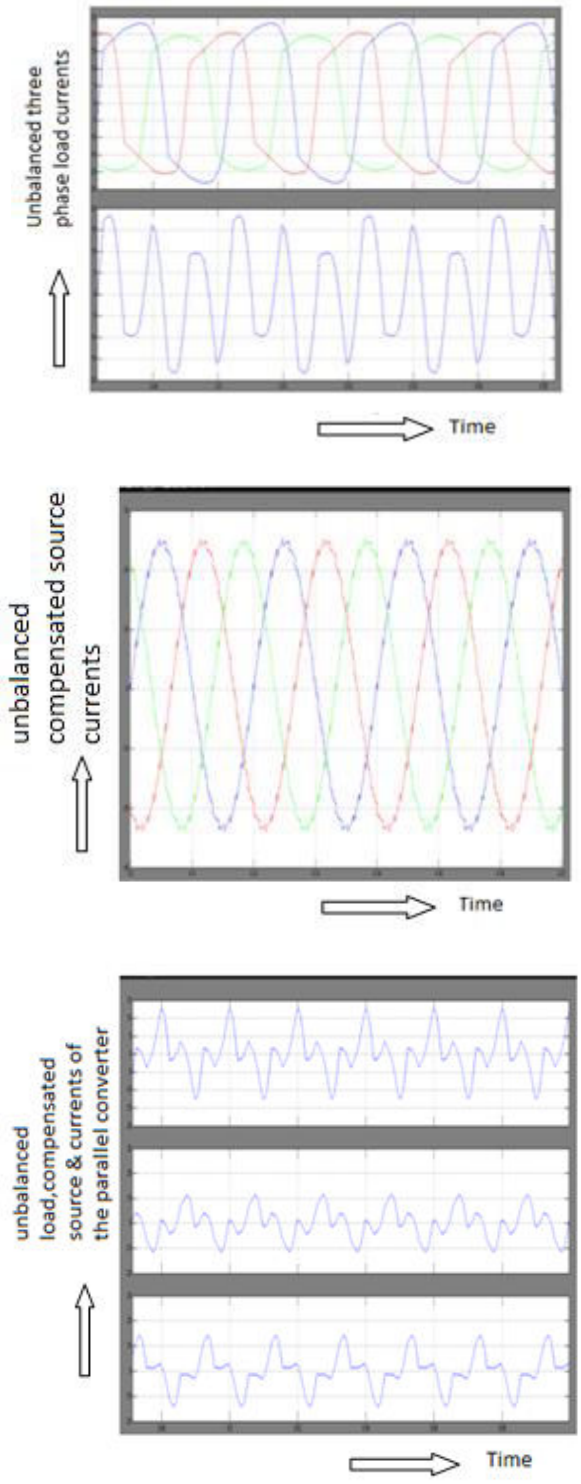
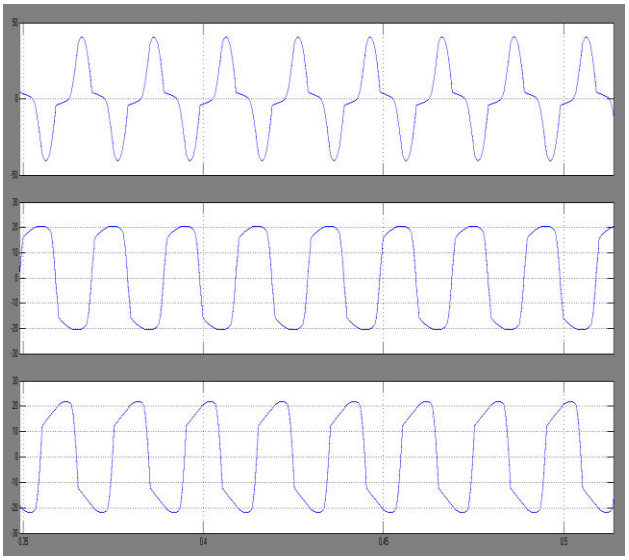


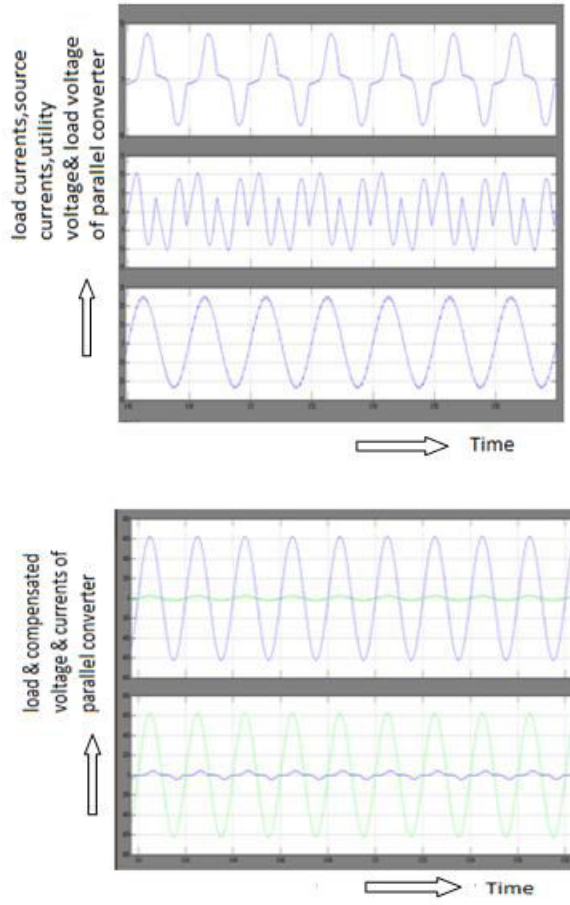
Fig.7 MATLAB/SIMULINK circuit for UPQC currents for unbalanced three-phase load



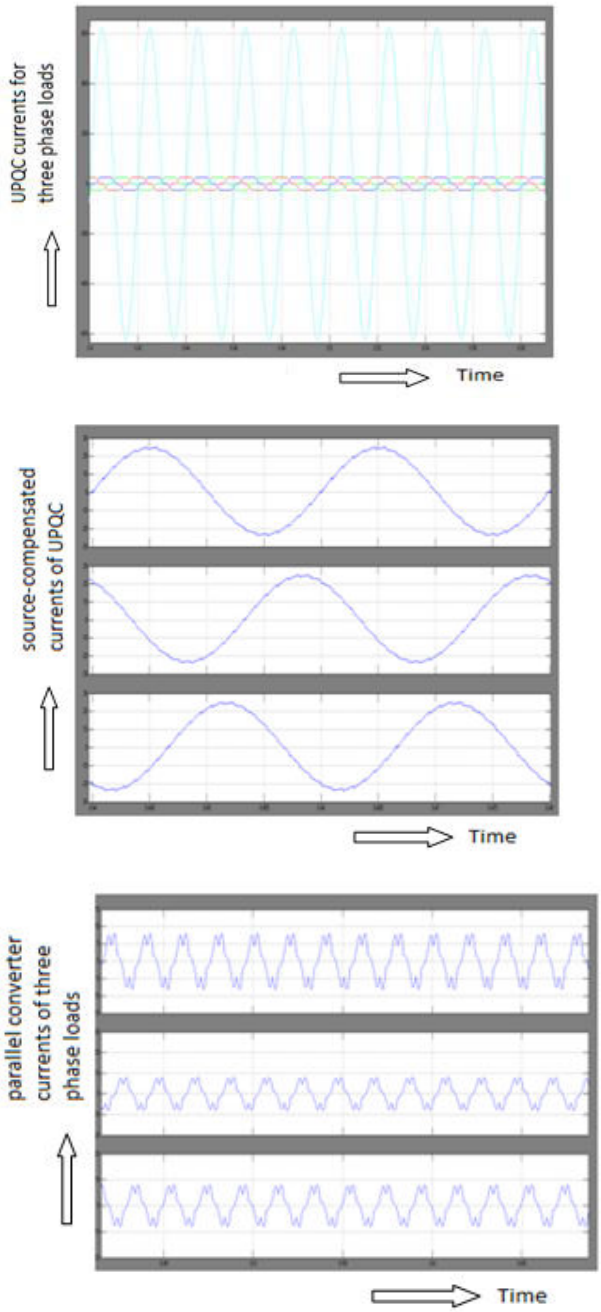
(a)

International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal





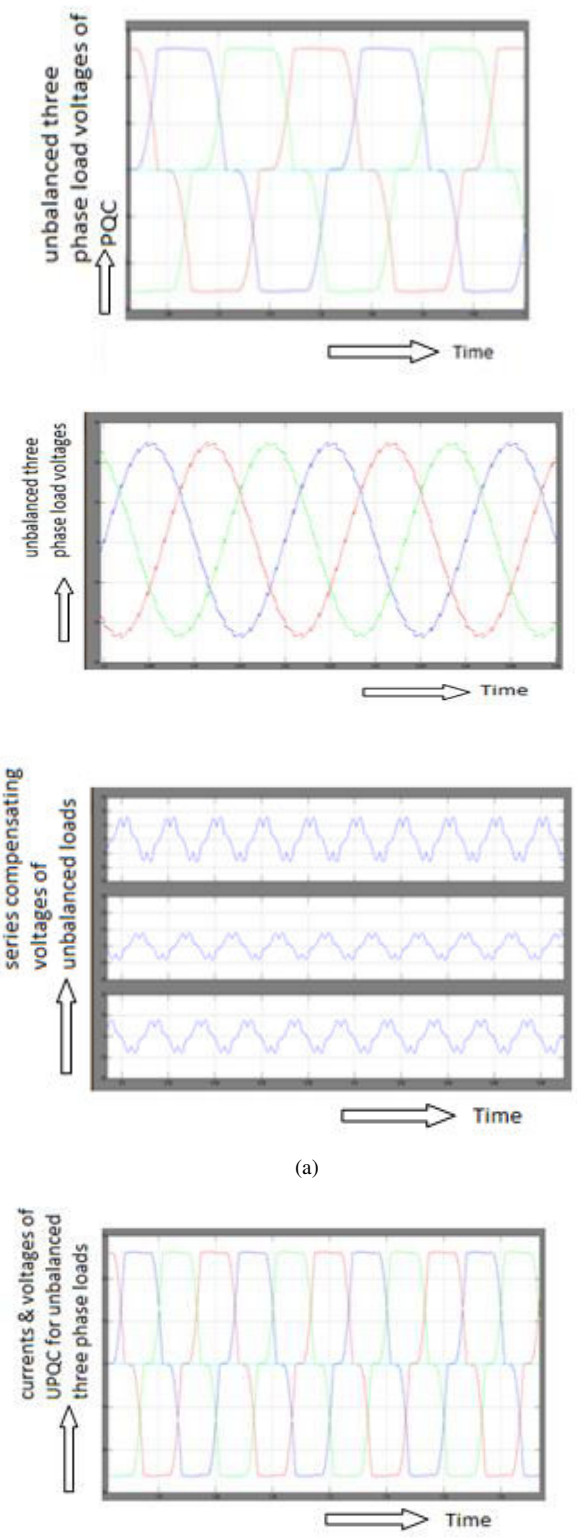
(b)

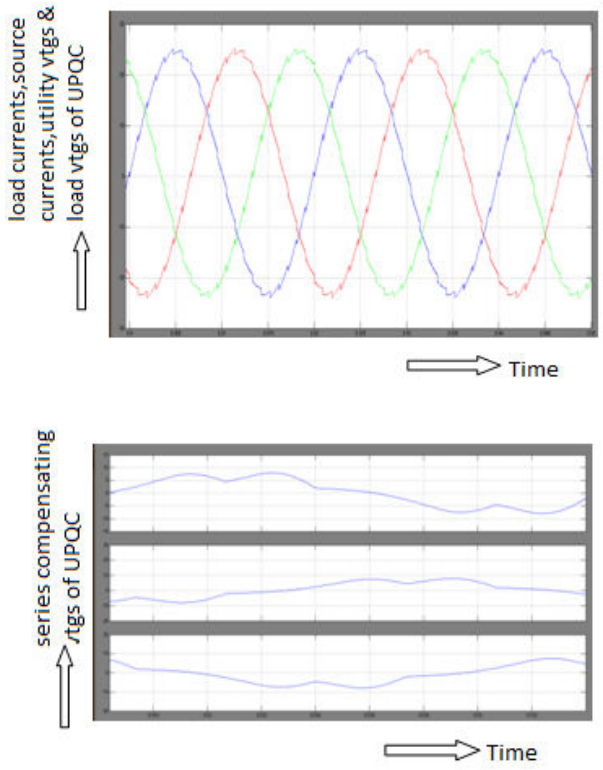


(c)

Fig.8.(a) UPQC currents for unbalanced three-phase load (1) (20 A/div, 5 ms/div): load currents (iLa,iLb, iLc)andiLn, compensated source currents (isa, isb, isc), and currents of the parallel converter (ica, icb, icc)andicn; (b) currents and voltages of phase"a" of the UPQC for the unbalanced three-phase load (2) (20 A/div, 100 V/div, 5 ms/div): load currents (iLa, iLb, iLc); currents of phase "a": loadiLa, parallel Converterica, and sourceisa; voltages and currents of phase "a": load currentiLa, source currentisa, utility voltagevsa, and load voltagevLa, (c) UPQC currentsfor three-phase load (1) (2.5 ms/div): load currents (iLa, iLb, iLc) (5 A/div), source-compensated currents (isa, isb, isc) (10 A/div), parallel converter currents(ica,icb,icc) (10 A/div).

International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal





(b)

Fig.9. Voltages of the UPQC under utility harmonics and unbalances for the unbalanced three-phase load (1): (a) utility voltages (vsa, vsb, vsc) (50 V/div, 2.5 ms/div), load voltages (vLa,vLb,vsL) (50 V/div, 2.5 ms/div), and series compensating voltages (vca, vcb and vcc) (50 V/div, 2.5 ms/div); (b) utility voltages (vsa, vsb, vsc) (50 V/div, 2.5 ms/div), load voltages (vLa, vLb, vsL) (50 V/div, 2.5 ms/div), and series compensating voltages (vca, vcb and vcc) (50 V/div,2.5 ms/div)

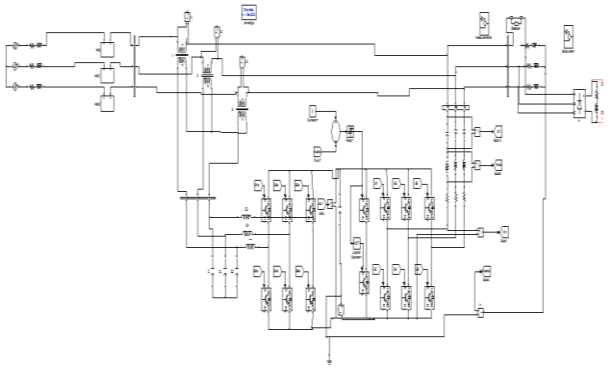
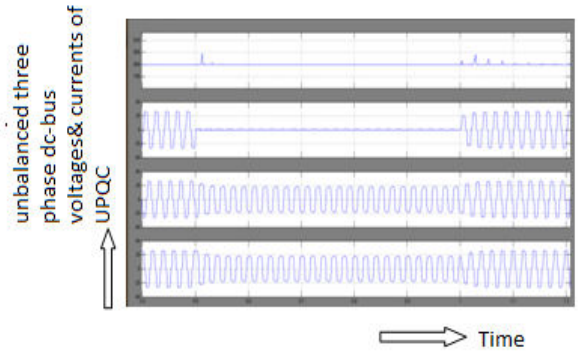
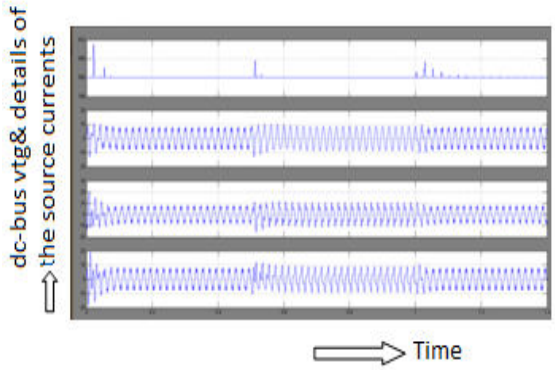


Fig.10 MATLAB/SIMULINK circuit for Voltages and current of the UPQC for the unbalanced three-phase load

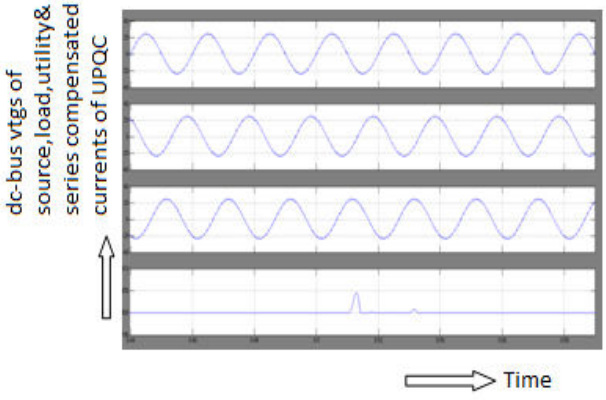
International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal



(a)

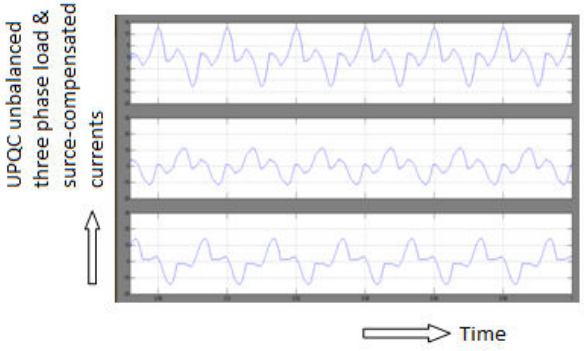


(b)



(c)

Fig.11. Voltages and current of the UPQC for the unbalanced three-phase load 1: (a) dc-bus voltage (Vdc) (100 V/div, 500 ms/div) and load currents (iLa, iLb,iLc) (20 A/div, 500 ms/div); (b) dc-bus voltage (Vdc) (100 V/div, 500 ms/div) and source currents (isa, isb, isc) (20 A/div, 500 ms/div); (c) dc-bus voltage (Vdc)(100 V/div, 5 ms/div) and details of the source currents (isa,isb,isc) after the first load transient (20 A/div, 5 ms/div)



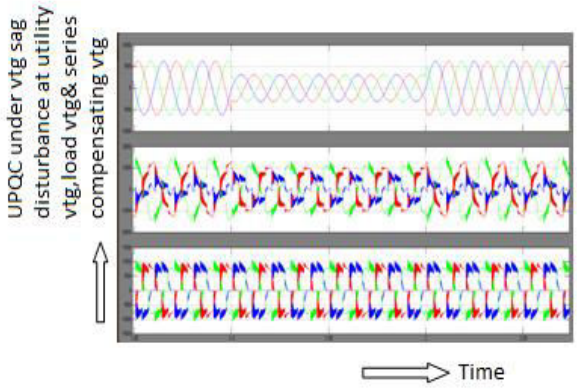
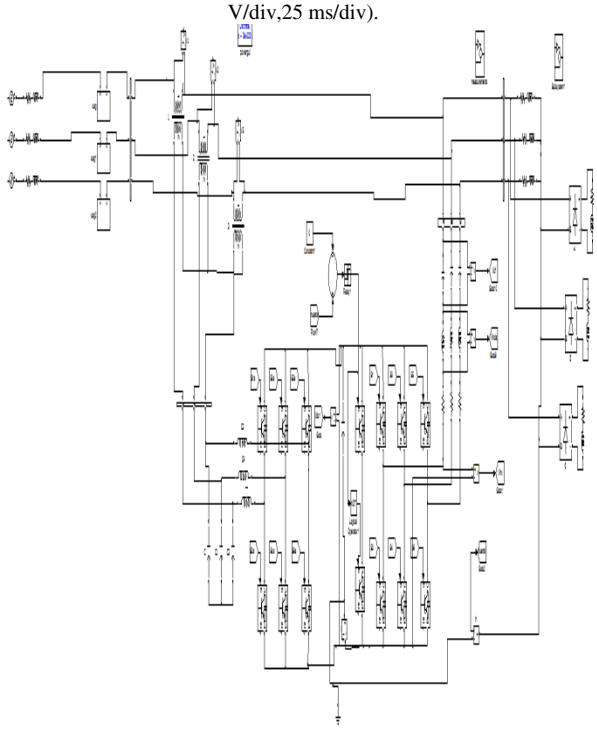
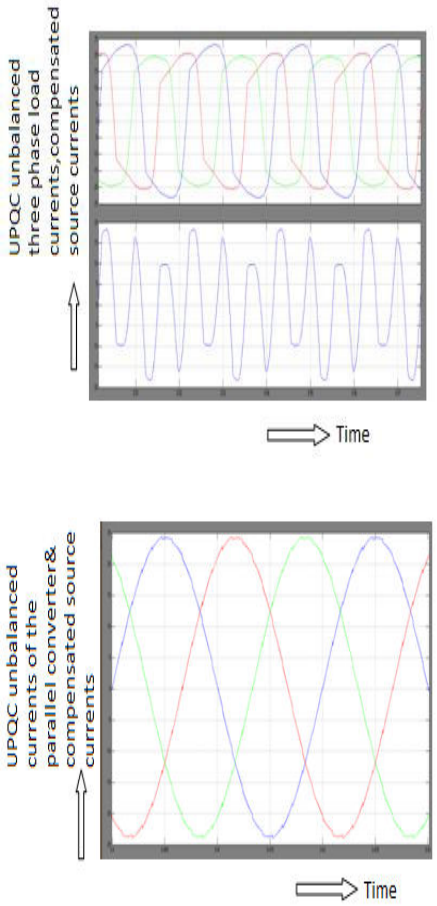


Fig.12. UPQC under voltage sag disturbance (phase "a"): utility voltage (vsa), load voltage (vLa), and series compensating voltage (vca) (200 V/div,25 ms/div).



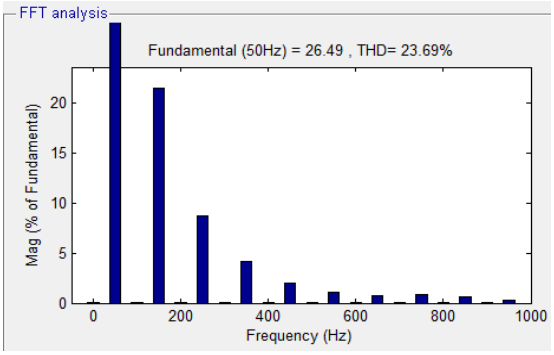
International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal

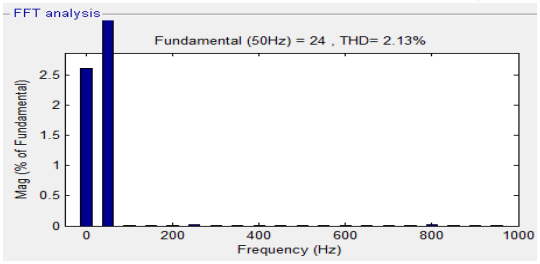
Fig.13 MATLAB/SIMULINL circuit of UPFC with Fuzzy Logic Controller



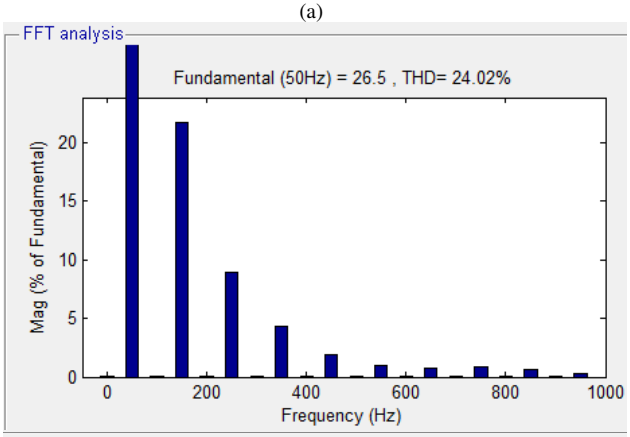
(a)

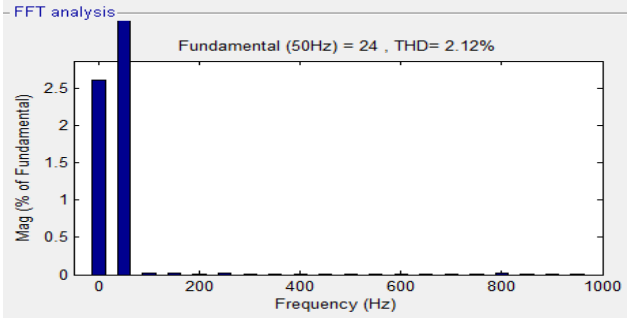
Fig.14 UPQC currents for unbalanced three-phase load with fuzzy logic controller (20 A/div, 5 ms/div): load currents (iLa,iLb, iLc)and iLn, compensated source currents (isa, isb, isc), and currents of the parallel converter (ica, icb, icc)andicn;



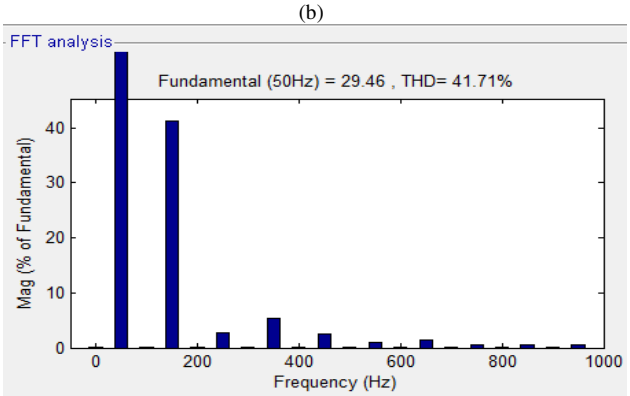


(a)

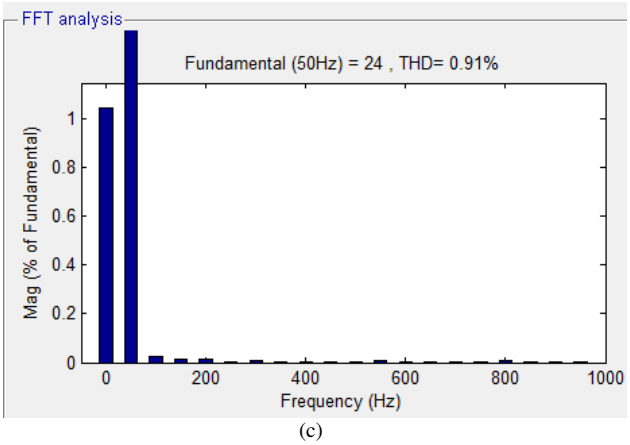




(b)



International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal



(c)

Fig.15. Harmonic spectra and THDs of voltage and current. (a) Voltages ofphase "a" for the unbalanced three-phase load 1: utility voltagevsa and loadvoltagevLa; (b) currents of phase "a" for the unbalanced three-phase load1: source currentisa and load currentiLa; (c) currents of phase "a"fortheunbalanced three-phase load 2: source currentisa and load currentiLa.

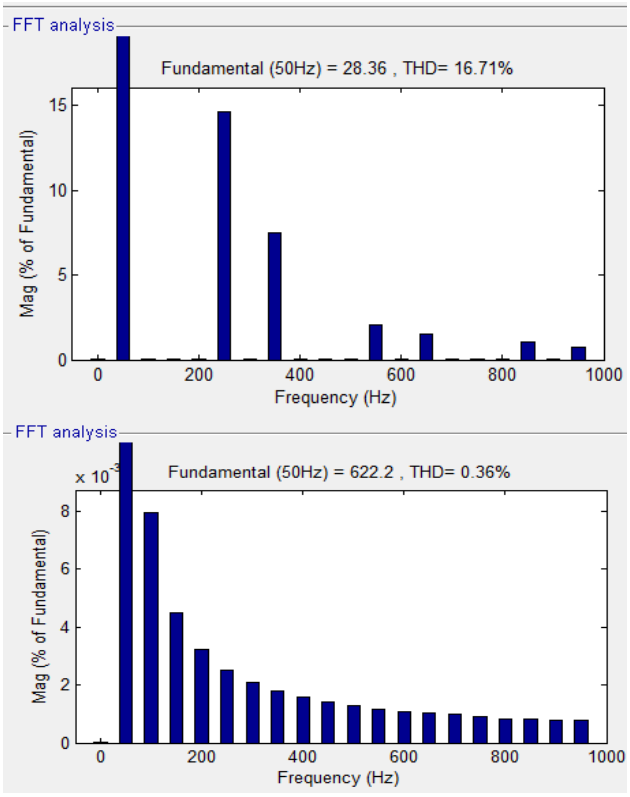


Fig.16 Source and load current THD plot

VIII. CONCLUSION

This project presents a practical and versatile application based on UPQC, which can be used in 3P3W, as well as 3P4W distribution systems. It was demonstrated that the UPQC installed at a 3P3W system plant site was able to perform universal active filtering even when the installed loads required a neutral conductor for connecting one or more single-phase loads (3P4W). The series–parallel active filtering allowed balanced and sinusoidal input currents, as well as balanced, sinusoidal, and regulated outputvoltages.

By using a dual control compensating strategy, the controlled voltage and current quantities are always sinusoidal. Therefore, it is possible to reduce the complexity of the algorithms used to calculate the compensation references. Furthermore, since voltage and current SRF-based controllers are employed, the control references become continuous, reducing the steady state errors when conventional PI controllers are used.

Based on digital signal processing static and dynamic performances, as well as the effectiveness of the dual UPQC were evaluated, validating the theoretical development.

REFERENCES

[1] Han Yingduo, Yan Gangui, Jiang Qirong, Huang Mincong. Electric Power in Information Society and FACTS & DFACTS [J]. Automation of Electric Power System, 2000, 24(19): 1-7.
[2]Wu Shan, Mei Tianhua, Gong Jianrong, GanDeqiang. Voltage Fluctuation and Flicker Caused by Distributed Generation [J]. Energy Engineering, 2006(4) : 54-58.
[3]Bai Qian. Mechanism of Voltage Regulation by Distributed Generation on Distribution Network [D]. Hebei: North China Electric Power University Baoding, 2007.
[4]ZhangGuorong. Research on Control Strategies of Unified Power Quality Conditioner (UPQC) [D]. Hefei: Hefei University of Technology; 2008.
[5] VinodKhadkikar, AmbrishChandra.UPQC-S: A Novel Concept of Simultaneous Voltage Sag/Swell and Load Reactive Power Compensations Utilizing Series Inverter of UPQC [J]. IEEE Transactions on Power Electronics, 2011, 26(9):2414-2425.
[6] Liang Zuquan, Shu Hongchun, Liu Zhijian, Yu Jilai. Completely Decoupled Direct Control Strategy of UPQC [J]. Electric Power Automation Equipment, 2009, 29(4): 27-31.
[7]WangYunling, Zeng Jie, Zhang Buhan, Mao Chengxiong. Dynamic Voltage Conditioner Based on Ultra capacitor Energy Storage System [J]. Power System Technology, 2007, 31(8): 58-62.
[8] P.Hoang, K.Tomosovic, "Design and an analysis an adaptive fuzzy power system stabilizer", Vol. 11, No. 2.June 1996.
[9] Momoh, X. W. Ma, "Overview and Literature survey of Fuzzy set theory in power systems,"IEEE Trans.on Power Systems, Vol. 10, No.3, Aug. 1995. pp. 1676-1690.
[10] M. Basu, S. Das, and G. Dubey, "Investigation on the performance of UPQC-Q for voltage sag mitigation and power quality improvement at a critical load point," IET Gen. Transmiss. Distrib, vol. 2, no. 3, pp. 414–423, May 2008.
[11] V. Khadkikar and A. Chandra, "A new control philosophy for a unified power quality conditioner (UPQC) to coordinate load-reactive power demand between shunt and series inverters," IEEE Trans. Power Del., vol. 23, no. 4, pp.2522–2534, Oct. 2008.
[12] M. Aredes and R. Fernandes, "A dual topology of unified power quality conditioner: The iUPQC," in Proc. 13th Eur.Conf. Power Electron. Appl., Sep. 2009, pp. 1–10.

[13] M. Brenna, R. Faranda, and E. Tironi, "A new proposal for power quality and custom power improvement: OPEN UPQC," IEEE Trans. Power Del., vol. 24, no. 4, pp. 2107–2116, Oct. 2009.
[14] V. Khadkikar and A. Chandra, "A novel structure for three- phase four-wire distribution system utilizing unified power quality conditioner (UPQC),"IEEE Trans. Ind. Appl., vol. 45, no. 5, pp. 1897–1902, Sep./Oct. 2009.
.