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Implementation of Low power and high speed 8 bit multiplier using 90nm technology

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Abstract
Vedic mathematics is an old mathematics which is more effective than other mathematic procedures. Vedic maths is utilized as a part of numerous applications, for example, hypothesis of numbers, compound duplications, squaring, cubing, square root and solid shape root and so on. Absolutely there are 16 sutras and 14 sub-sutras in Vedic maths. Among those sutras, just 3 sutras and 2 sub-sutras are utilized for augmentation. Multiplier is a very important part of a microprocessor as multiplication is performed continuously in all calculative procedures. This paper is in importance of a 8-bit multiplier designed in 90 nm technology. Urdhva-Tiryakbyham is the sutra that is used for multiplication in Vedic mathematics. Actualizing the different scientific operations utilizing Vedic Mathematics causes us accomplish better speed, bring down unpredictability and higher execution.[2] The technique used is Gate Diffusion Input (GDI) which is a more refined way to design a circuit which less complex than circuits designed by other techniques.
Index Terms: *Vedic Multiplier, Urdhva-Tiryakbyham, Gate Diffusion Input, 90 nm technology.*

1. Introduction

In this fast pacing world of advancing science and technology, when we talk about vedic multipliers, a lot of research has been done and as a matter of fact already been going on. This is because of the importance of results that researchers have gotten but there is always a scope. In this paper 8-bit vedic multiplier is designed using GDI technique in 90 nm technology. The most vital requirement of any processor would be Speed, Area and power which are also the three pillars of VLSI. The design Proposed in this paper would give us a circuit which will have high speed, reduction in delay and it would consume less power. The circuit made will be performing in an improved manner because of the usage of vedic mathematics and gate diffusion input.

When we talk about processors like FFT, DSP convolution, IDFT and many others, multiplier is considered as the the foundation stone. In Laymen language a multiplier is something that would give us multiple outputs when lesser inputs are provided or in other words, a number by which the other number is multiplied. For every processor to have higher speed, a high speed multiplier is suggested. The higher the speed of the multiplier would be , the more efficient will the processor worked out to be. Research has shown that whenever we switch to vedic multiplier, all these concerns can be satisfied.

The most popular sutras of vedic mathematics are Urdhva-Tiryakbhyam and Nikhilam sutra (names derived from Sanskrit) but when it comes for the multiplication or in this case use of a

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multipier, the most appropriate sutra to be used will be the UT (Urdhva-Tiryakbhyam) sutra. Hence in this paper only this sutra is used and discussed. [1]

In a vedic multiplier using GDI, vedic multiplication comprises of AND gates, half adders and full adders. Vedic multiplication requires less processing time for the execution that‟s why it has been used here as it is a sturdy way of multiplication. It makes the use of less number of transistors in comparison to C-MOS. Realizing these functions using CMOS requires 6-12 transistors. But the same functions are very easy to implement using GDI method and require only two transistors per function.

2. Technologies Used

Gate Diffusion Input (GDI)

GDI can be described as a method of less-power circuit integration. With this method we can reduce power consumption, propagation delay, and area with a less complex circuit. If we compare the traditional CMOS design and the GDI circuit, we can easily see the difference in terms of power consumption. The layout area, number of devices, delay, and power dissipation are the factors that are directly affected as we use gate diffusion input logics.[6] Technology adaptability, better design, and precomputing amalgamation are some of the issues that have come into light, presenting the pros and cons of GDI to other techniques. The paper shows a upgraded low-power design technique that solves the major problems mentioned in the introduction. The GDI method permits the execution of bulks of complicated logic functions by the use of only two transistors.

The basic GDI cell can be seen and the basic functions of a GDI cell can be understood.[6]

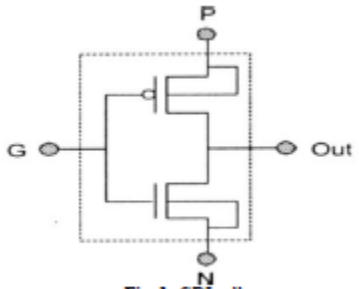

Fig. 1: GDI cell

Functions of Gate Diffusion Input

The GDI is built on the usage of an uncomplicated cell like structure above. The fundamental figure shows us a CMOS inverter, but we can observe some major differences.

1) Cell shown in fig.1 has 3 inputs - G , P and N where „G‟ being the common gate to both p and n type Mosfets, „P‟ referring to the I/P of p-MOS and „N‟ being input of n-MOS.

2)P-MOS and N-MOS are connected to P and N (respectively), so it can be inconsistently favourable with a CMOS inverter.

The designed circuits were based on the F1 and F2 functions in this paper. The reasons for this are :

1) F1 and F2 can be described as complete logic families [allow registration of 2 I/P functions].

2) F1 as a GDI function that can be registered as a quality CMOS process{P}, where the n-MOS is evenly biased.

Table 1: Logic Functions of GDI cell for Different inputs

N	P	G	OUT	Function
0	Y	X	X'Y	F1
Y	0	X	X'+Y	F2
1	Y	X	X+Y	OR
Y	0	X	XY	AND
Z	Y	X	X'Y+XZ	MUX
0	1	X	X'	NOT

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90 Nano-Meter Technologies

The 90 nanometer integration describes to a standard of CMOS technology founded during time frame 2004-2005 by major semiconductor companies like intel, IBM etc. 90nm uses state of the art technology that can be used in the integration of the circuit. Technologies like 180nm and 45nm goes by the same integration standards. Also these numbers are not randomly assigned but are decided by dividing the previous number by the square root of 2 (because 2 is neither too small nor too big). Different technologies are being used today and the transistor size is shrinking day by day to lower the cost of production of a chip and it is also cheaper to make it. It is even estimated that the size will even shrink to 4nm(approx.) by the year 2020."

Tool Used: Tanner EDA 14.1

The tool used for the simulation of the circuits is Tanner EDA 14.1. The simulation is done using T-spice. The circuit schematics are presented in further stages.

Algorithms Used for the 4x4 Bit Vedic Multiplier

1. A0 = X0Y0
2. A1 = X1Y0+XoY1
3. A2 = X2Y0+X1Y1+X0Y2+X0X1Y0Y1
4. A3 = X3Y0+X2Y1+X1Y2+X0Y3+carry from A2.
5. A4 = X3Y1+X2Y2+X1Y3+carry from A2+carry from A3.
6. A5= X3Y2+X2Y3+carry from A4+carry from A3.
7. A6= X3Y3+X1X2Y1Y2+carry from A4.
8. A7= carry from A6.

The 4x4 Vedic multiplier is designed from UT sutra and carry-skip method for the partial product addition. In a vedic multiplier, the carry from each partial product addition is transferred to the next bit. This depicts the vertical and crosswise method of finding o/p value of the vedic multiplier.[3]

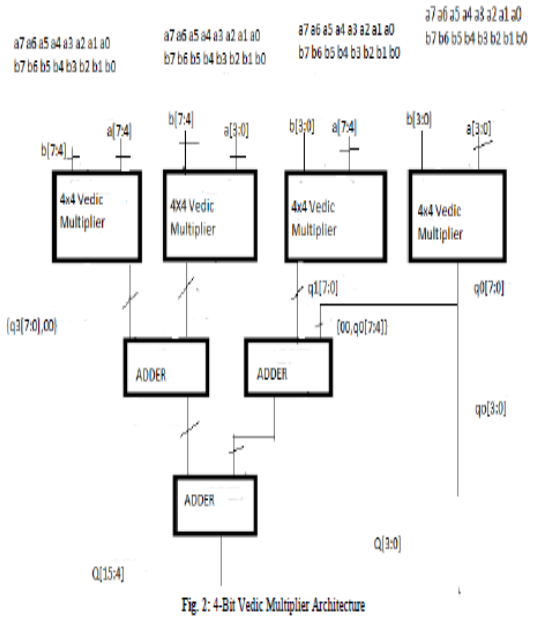

Fig. 2: 4-Bit Vedic Multiplier Architecture

These equations come handy in the 4-bit multiplier but when we move on to 8-bit multiplier the equations will be sixteen which is double the UT equations we use for the 4x4 vedic multiplier. This is done in the similar fashion as it is showcased above. As seen in Fig.2, the 4x4 usually made up of Adders which is further discussed in the paper.[4]

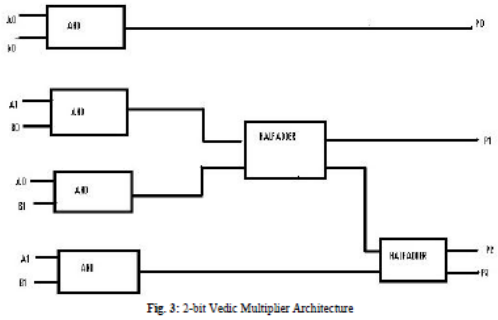

Fig. 3: 2-bit Vedic Multiplier Architecture

It is a 2 bit multiplier which is based on the Urdhvatiryakbyham sutra. This 2-bit vedic multiplier comprises of 4 „AND" gates {each having two I/Ps}. Also it comprises of a „Half Adder" which is explained ahead.

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This is the base of our 8 bit vedic. It is also the prime element of the 4-bit multiplier. All the the other elements that are used in the formation of the 8-bit multiplier are further explained so that we can get a clear picture about the integration of the "8-bit Vedic Multiplier."

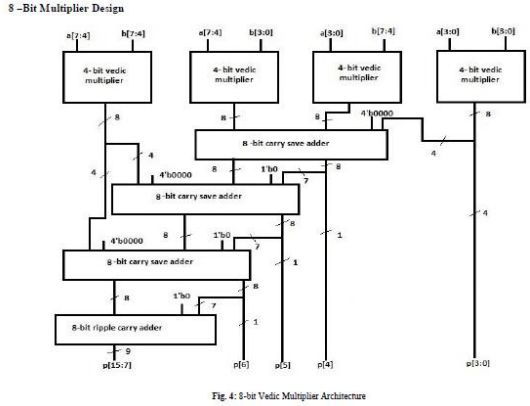

Fig. 4: 8-bit Vedic Multiplier Architecture

Elements Used in the 8-bit multiplier are

1. AND Gate

The AND gate is a fundamental digital gate. It comprises of two I/Ps and one O/P. These can be explained with the help of a truth table below. Here in this paper, AND gate is used in the circuit integration of carry select adder (element of 8 bit vedic multiplier) as shown in Fig.4 and also used in the integration of the 2 bit vedic multiplier. The operations of the AND gate as in table.2 can be explained by the means of a truth table.

An Adder is any circuit is an integral part. The case is certainly not different with multiplier. Especially with the vedic multiplier. In Half adder we add two I/P bits but the carry is neglected and the result is given just on the basis of addition of 2 bits.[4] The major difference that comes in this circuit to the conventional half adder circuit is that this is made using the Gate Diffusion Input technique which makes the and integration of circuit much easier and much more efficient. The Half adder circuit is shown below in fig.5.

2. HALF Adder

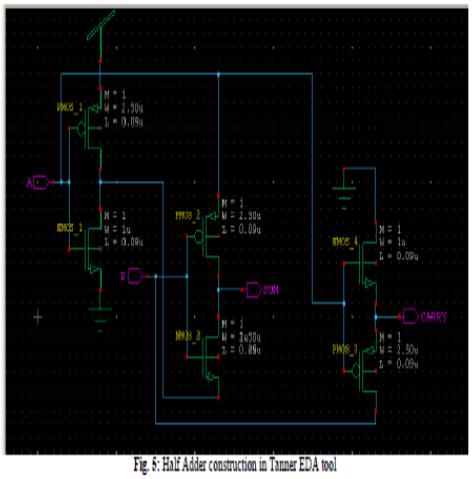

Fig. 5: Half Adder construction in Tanner EDA tool

3."FULL Adder

Similar method of construction is taken onto the full adder which is one of the important elements Vedic Multiplier, be it a 4x4 or 8x8. The purpose of the Full adder is to add the nos. (binary) and also accounting the carrys in and out. Here the full adder is framed into circuit using the GDI logics like in fig.6. The advantages that GDI provide over other conventional techniques

has been discussed already in the paper. Here in this circuit integration, A and B are given in as I/Ps. Also Cin is recognised as carry in and outputs contain Cout and Sum as outputs.[1] All the values of the gates and devices in the circuit have already been updated according to the 90nm technology standards.

The schematic Diagram of the full adder using GDI in 90nm technology can be described as shown in the figure below:

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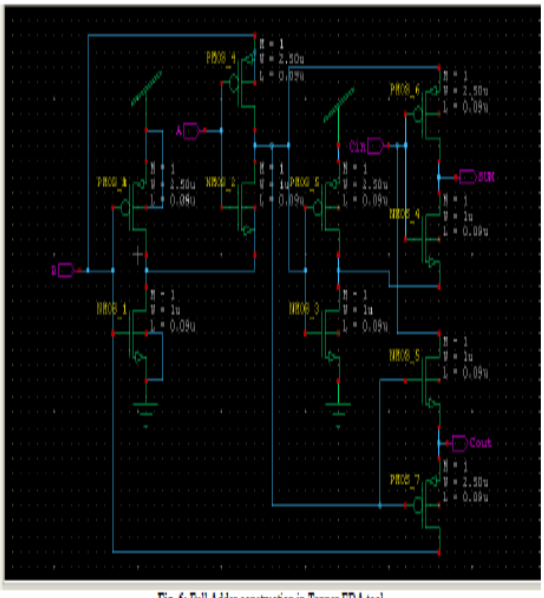

Fig. 6: Full Adder construction in Tanner EDA tool

4. Carry saves Adder

The carry save adder in this 8 bit vedic multiplier plays a vital part in the integration of the multiplier. The elements are used in this demonstration of the carry save adder are AND gates, and XORs with GDI logics. Also the use of 90 nm makes the configurations a lot cleaner when it comes to the hardware. The AND gate is formed using 3 NORs as shown in Fig.7. So the demonstration of the CS Adder is also done on Tanner EDA 14.1.

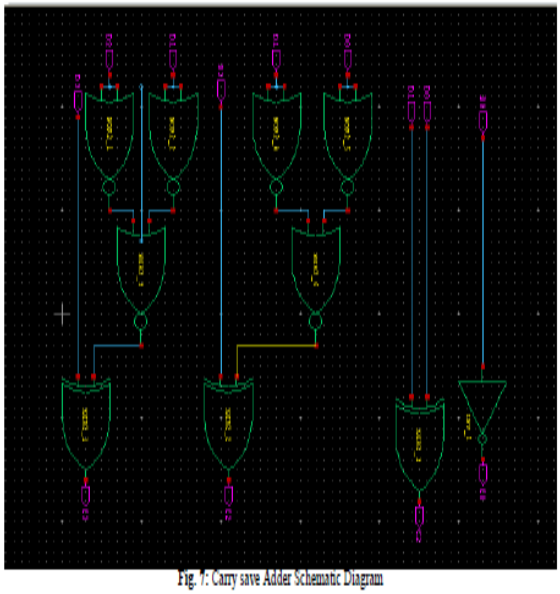

Fig. 7: Carry save Adder Schematic Diagram

3. Result

The implementation of the 8-bit Vedic Multiplier and simulation using GDI technique in 90nm technology shows us the results and observations using a comparative analysis. The parameters taken in focus were power consumption, transistor count, efficiency and propagation delay.

The results found can be shown in Table-3.

Table 3: Results based on Comparative Analysis and Simulation

Parameters	180nm	90nm(Result)GDI
Power Consumption	1.414mw	Reduced to 42-45%.
Transistor count	2110	1850
Efficiency	Less.	More efficient.
propagation delay	0.95	0.775

4. Conclusion

After doing the construction on Tanner EDA 14.1 and simulation of all the elements(circuits) present in the 8-bit vedic multiplier using T-spice. Also after doing the comparative analysis of the 2,4 and 8-bit

Vedic multipliers using GDI technique in 90nm technology to the conventional methods or techniques, a few observations are achieved.

With the use of the GDI logics in all the circuital work it is feasible to say that just because using the GDI technique over the conventional or old-school techniques, the power consumption is reduced by 42-45% which makes a huge difference. Now in terms of transistors used and layout area aswell after the comparative analysis which was reached by comparing our multiplier using 90nm to the other major technologies such as 180nm . In terms of no. of transistors used in 180nm is about 2110 but when we take the 8-bit vedic multiplier using GDI in 90nm technology, we achieve an appropriate and balanced no. of transistor count which is 1850. Hence we get a better working multiplier on the top of appropriately cleaner setup.

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