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# IMPLEMENTATION OF 1-BIT LOW POWER FULL ADDER USING CADENCE TOOL

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## ABSTRACT

This paper presents a novel low-power majority function-based 1-bit full adder that uses MOS capacitors in its structure. The power consumption and general characteristics of an adder are then compared against low power adders, the Transmission Gate fullAdder (TGA) and the conventional CMOS full adder. The circuits simulated using CADENCE tool 180nm CMOS process technology. Analysis of performance and efficiency of 1-bit full adder cell designs is carried out for different parameters like average power, supply voltage and transistor count is done. The average power for CMOS technology for 180nm is 209.2uW and for Transmission gate technology for 180nm is 164.4uW. It is observed that within a given logic style, as the technologydecreases the average power decreases with decrease in the area for a constant supply voltage of 5V. It is observed that less power is consumed by transmission gate based 1-Bit full adder than the conventional CMOS 1-Bit full adder.

**Keywords:** Low-power Full-adder, Low-power CMOS design, Transmission Gate fullAdder.

## 1. INTRODUCTION

With the continuously increasing chips complexity and number of transistors, circuits power consumption is growing as well. Low power circuits have been major design challenge in VLSI technology. Technology enhancements reduce the area for a single chip and increase the number of transistors on a single dice. High number of transistors on single chip leads to high power dissipation. The most conventional one is complementary CMOS full-adder (C-CMOS). It is based on regular CMOS structure with pull-up and pull-down transistors and has 28transistors.

The Transmission Gate Full-Adder (TGA) is proposed. It is based on transmission function theory and transmission gates and has 16 transistors. Transmission gates consists of a PMOS

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transistor and an NMOS transistor that are connected in parallel.

In this paper a novel full adder circuit is introduced which designed by using inverters and transmission gate. This full adder having simple structure and reduced power consumption in comparison to another designs. The reduction in power consumption due simple structure of circuit and decreased number of transistors used in the circuit.

## 2. LITERATURE REVIEW OF FULL ADDER

The most conventional one is complementary CMOS full-adder (C-CMOS). It is based on regular CMOS structure with pull-up and pull-down transistors and has 28 transistors. Another existing system Transmission Gate Full-Adder (TGA) presented in [8] contains 20 transistors. The Transmission Gate Full-Adder (TGA) is proposed. It is based on transmission function theory and transmission gates and has 16 transistors.

The circuit diagram of a 3-bit full adder is shown in the figure. The output of XOR gate is called SUM, while the output of the AND gate is the CARRY. The AND gate produces a high output only when both inputs are high. The XOR gate produces a high output if either input, but not both, is high. The truth table of 3-bit full adder is given. The 3-bit full adder circuit has a provision to add the carry generated from the lower bits.

The expression for SUM and CARRY is given by,

SUM=A $\oplus$ B $\oplus$ Cin = A'B'Cin' + A'BCin' +AB'Cin' +ABCin

CARRY= AB + Cin (A $\oplus$ B) = AB + ACin + BCin = AB + Cin(AB' + A'B)

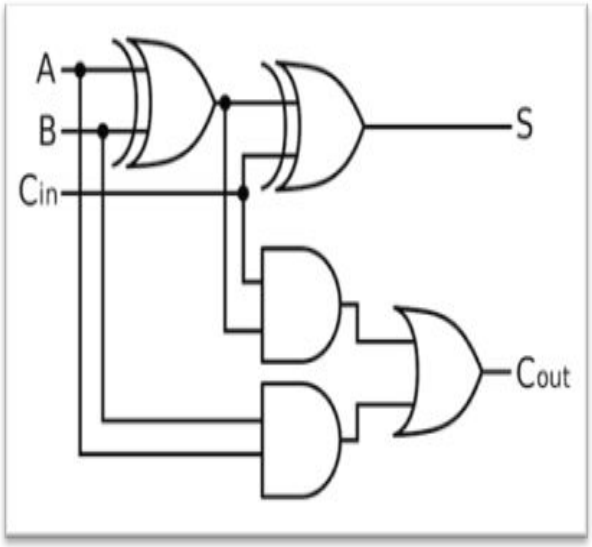


**Fig 1. Full Adder Circuit**

**Table1: Full Adder Truth Table**

| Inputs | | | Outputs | |
|---|---|---|---|---|
| A | B | $C_{in}$ | Sum | Carry |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

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## 3. EXISTING METHOD

**Conventional CMOS Full Adder:**

The 1-bit conventional CMOS full adder cell is shown in Fig2. The Complementary MOS Logic Style consists of Pull-Up Network (PUN), which has PMOS transistors and the Pull-Down Network (PDN), which consists of NMOS transistors. The Pull-Up Network connects the output of the gate with Vdd whenever the output of the gate is high. The Pull-Down Network connects gate output and GND when the gate output is low. This logic style consists of 28 transistors.

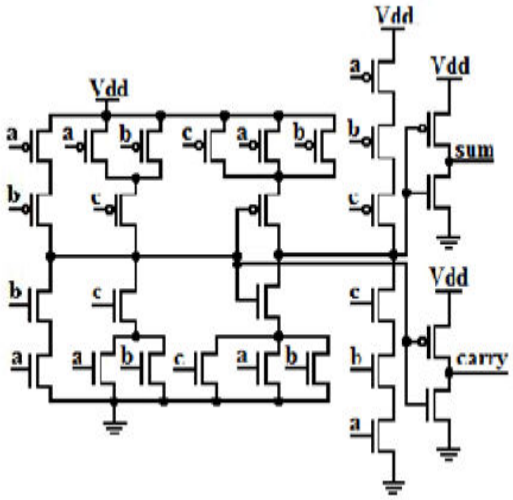


**Fig 2:1-Bit Conventional CMOS Full Adder**

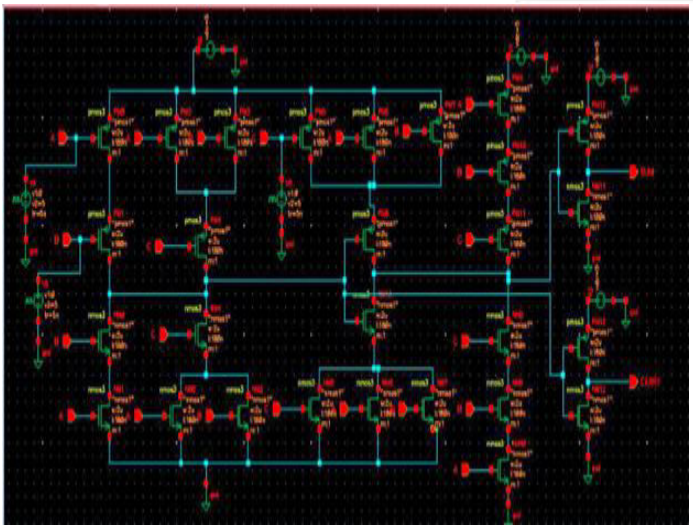

**Fig 3: 1-Bit Conventional CMOS Full Adder in Schematic Editor**

## 4. PROPOSED METHOD

**Transmission Gate Full Adder:**

The TG full adder [8], shown in Fig. 3, is based on transmission gates and introduced for its low power dissipation [4]. As in the case of the LP circuit, cascading full adders leads to an overall propagation delay roughly proportional to, which becomes excessive for long chains of full adders. This drawback is solved in the TG drivcap [6]. Output buffers which interrupt the transmission gate chain when cascading full adders are added.The use of transmission gates enables the circuit to have high speed and low power dissipation.

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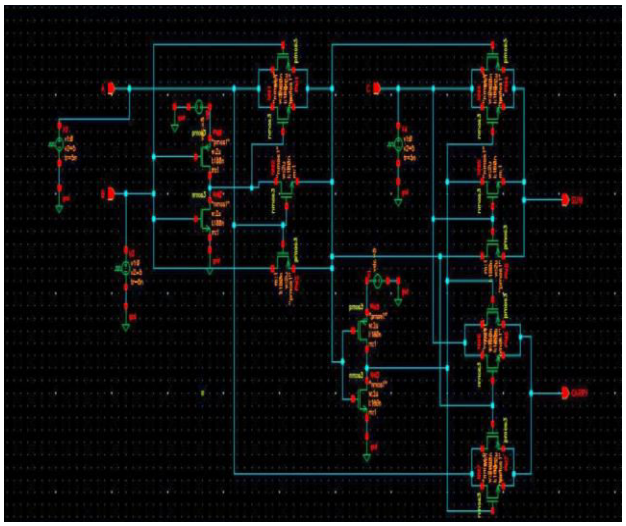

**Fig 4: 1-Bit Transmission Gate Full Adder in Schematic Editor**

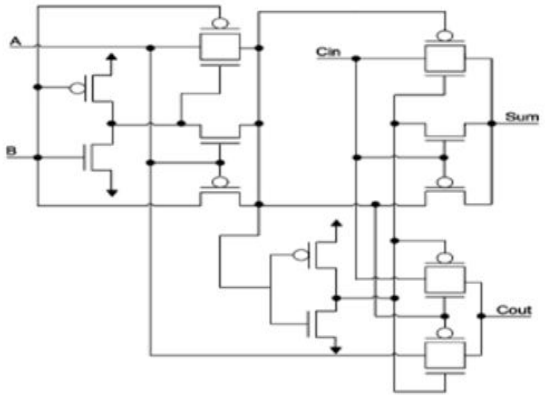


**Fig 5: 1-Bit Transmission Gate Full Adder**

## 5. METHODS OR TECHNIQUES USED

The Cadence tool kit consist of several programs for different applications such as schematic drawing, layout, verification, and simulation.Cadence is a leading Electronicdesign automation (EDA) software.Cadence Virtuoso Analog Design is used for design and simulation which is the advanced design and simulation environment for the Virtuoso Platform.

## 6. SIMULATION RESULT

Simulation results are performed by SPECTRE in Virtuoso, Cadence at 180nm CMOS process with the 5V of input voltage and supply voltage. The proposed circuit 1-Bit TransmissionGate Full Adder evaluated and compared to the 1-Bit Conventional CMOSFull Adder circuit. The power obtained of the designs are summarized in the Table 2 for 5V voltage and loads at a fixed input rise and fall time of 5nm. The simulation analysis is carried out with three inputs (A, B, C) and two outputs (Sum and Carry) of Full Adder.

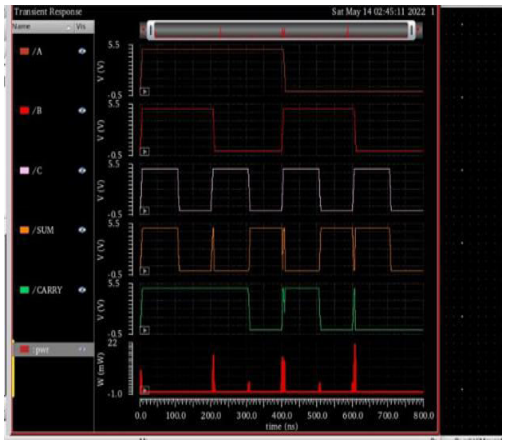


**Fig 6: Output Waveforms of Full Adder**

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Table2: Simulation Result

| S.No | Parameter | CMOS Full Adder | TGL Full Adder |
|---|---|---|---|
| 1. | Technology | 180nm | 180nm |
| 2. | Supply Voltage | 5V | 5V |
| 3. | Power | 209.2uW | 164.6uW |

## 7. CONCLUSION

Design and simulation of optimized low power 1-bit CMOS and TGLfull adder has been done at 180nm Technology.Low power consumption is preferred in V.L.S.I systemsowing to theirgreater reliability. Cadence virtuososimulations have been performed to evaluate the fulladder cell. In this paper, theperformance of 1-Bit full adder using CMOS andTransmission gate logic styles are compared and analyzed for the parameters like average power supply voltage,transistor count. Also, it is observedthat for one given technology the transmission gate based 1-Bit adder has lower average power, less transistor countand smaller area than the CMOS based 1-Bit full adder circuits.

## 8. FUTURE SCOPE

In Future, there is Scope for an area efficient, low power and high speed 1-bit full adder by reducing number of transistors such as 10T, 8T, 6T.By the reduction in transistors can produces full swing out signals, which implies this adder has a good driving capability.A prototype of this proposed cell(10T) is built using a 0.6 um CMOS process with single polysilicon and double metal interconnections. Therefore, the cell size of 10T cell is smaller than TGL (the saving in area is equal to 40%)and CMOS cell (the saving in area is equal to 50%).

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