International Journal For Recent Developments in Science & Technology
Crossref
A Peer Reviewed Research Journal
2581-4575

Revolutionizing ALUs: A Deep Dive into Majority Logic Gate Integration

M. Nagasri[1],Komatireddy Uday Kumar Reddy[2],Ankireddygari Muralidhar Reddy[2],Sheeraboina Deepika[2],Veeramalla Manideep[2],Parsewar.Surya Chaitanya[2]

[1]Assistant Professor,[2]UG Student,[1,2]Department of Electronics & Communication Engineering

[1,2]Malla Reddy Engineering College and Management Sciences,Kistapur,Medchal,501401, Telangana

The design of Arithmetic Logic Units (ALUs) is a critical aspect of modern digital circuitry, influencing the overall performance of processors. This study introduces a novel approach to ALU design by employing Majority Logic Gates (MLGs) instead of traditional AND, OR, and XOR gates. The conventional ALU systems typically rely on a combination of these gates, leading to increased complexity, higher power consumption, and larger silicon footprint. The drawbacks of conventional ALU designs include limited scalability, longer critical paths, and a greater number of transistors, contributing to elevated production costs. In contrast, the proposed system utilizes Majority Logic Gates to perform logical operations, taking advantage of their inherent efficiency and reduced transistor count. The utilization of MLGs enables a streamlined and compact ALU design, enhancing both performance and energy efficiency. The study evaluates the proposed ALU's functionality, efficiency, and performance metrics through simulations and compares the results with traditional ALU designs, demonstrating the viability and advantages of the Majority Logic Gates-based approach in ALU design. This research contributes to the ongoing efforts to optimize digital circuitry for improved computational capabilities in a more resource-efficient manner.

Keywords: logic gate,Arithmetic logic unit,Integration.

1. INTRODUCTION

Optimizations in VLSI have been done on three factors: Area, Power and Timing (Speed).Area optimization means reducing the space of logic which occupy on the die. This is done in both front-end and back-end of design. In front-end design, proper description of simplified Boolean expression and removing unused states will lead to minimize the gate/transistor utilization. Partition, Floor planning, Placement, and routing are perform in back-end of the design which is done by CAD tool .The CAD tool have a specific algorithm for each process to produce an area efficient design similar to Power optimization. Power optimization is to reduce the power dissipation of the design which suffers by operating voltage, operating frequency, and switching activity. The first two factors are merely specified in design constraints but switching activity is a parameter which varies dynamically, based on the way which designs the logic and input vectors. Timing optimization refers to meeting the user constraints in efficient manner without any violation otherwise, improving performance of the design.Quantum-dot cellular automata (QCA) are an attractive emerging technology suitable for the development of ultra dense low-power high-performance digital circuits. Quantum-dot cellular automata (QCA) which employs array of coupled quantum dots to implement Boolean logic function. The advantage of QCA lies in the

extremely high packing densities possible due to the small size of the dots, the simplified interconnection, and the extremely low power delay product. A basic QCA cell consists of four quantum dots in a square array coupled by tunnel barriers. Electrons are able to tunnel between the dots, but cannot leave the cell. If two excess electrons are placed in the cell, Coulomb repulsion will force the electrons to dots on opposite corners. There are thus two energetically equivalent ground state polarizations can be labeled logic "0"and "1".The basic building blocks of the QCA architecture are AND,OR and NOT. By using the Majority gate we can reduce the amount of delay.i.e by calculating the propagation and generational carries. Quantum dots are semiconductors confined in all three dimensions of space or alternatively, it can be noted that Quantum dot is a simple charge container and it is three dimensionally confined [8]. The promising alternative of CMOS paradigm is the Quantum dot cellular Automata (QCA) which is used to represent the information in binary M' and binary 'O' in terms of electronic charge configuration. In 1993, C. S. Lent et al. first introduced the theoretical Quantum dot Cellular Automata [3] and in early 1999, C. S. Lent et al. described the experimental approach to design QCA cell with GaAs [8]. The dynamic behaviour of QCA was discussed with the help ofthe hart tree approximation [4], Quantum mechanics is also involved in finding out the cell size and dot radius of a single QCA cell. Hence, QCA became research interest to establish as strong CMOS alternative. During last decades, in nanotechnology era, an exhaustive research has been carried out in this domain. QCA is still in infancy stage, needs lots ofstudy for QCA logic circuit design. The low power reversible logic circuit design, tile based logic circuit design as well as its defect analysis are prime problem domain. The ternary computing with QCA is most challenging task in this domain since no such improvement is noticed. The multivalued computing, specifically ternary computing is an emerging domain of research due the potential advantages like greater data storage capability, faster arithmetic operations, better support for numerical analysis, application ofnon-deterministic and heuristic procedures, communication protocol and effective solution for non-binary problems. Nano-scale logic circuit fabrication is suffering from defects that may occur during fabrication. It is also noticed that QCA fabrication is suffering from high probability of defect. It was reported in several proposals [59-60, 63-70] that defects are considered mainly on deposition phase.

2. LITERATURE SURVEY

The evolution of electronic information technology (IT) and communications has been mainly possible by continuous progress in silicon-based Complementary Metal Oxide Semiconductor (CMOS) technology. This continuous progress has been maintained mostly by its dimensional scaling, which results in exponential growth in both device density and performance. The reduction in costperfunction has steadily been increasing the economic productivity with every new technology. In addition to its scalability, the unique device properties such as high input resistance, self -isolation, zero static power dissipation, simple layout and process steps have made CMOS transistors as the main components of CMOS integrated circuits (ICs). However,the dimensions of CMOS transistor shrinks and approaches towards the close proximity between source and drain, which reduces the ability of the gate electrode to control the potential distribution and the flow of current in the channel region. Thus avoiding further reduction size.

Dimensional scaling of CMOS transistors is reaching their fundamental physical limits [24-25]. Therefore, research has been actively carried out to find an alternative way to continue to follow

Moore's law. Among these efforts, various kinds of alternative memory and logic devices, so called "Beyond CMOS Devices," have been proposed [8]. These nano-devices take advantage of the quantum mechanical phenomena and ballistic transport characteristics under lower supply voltage and hence low power consumption. These devices are expected to be used for ultra-high density integrated electronic computers due to their extremely small size.

Nano-wire Field-Effect Transistors (NWFETs) have drawn promising attention and have been considered an alternative to continue CMOS scaling, since their nonplanar geometry provides superior electrostatic control of the channel than the conventional counter parts. The increasing attention in Nano-wire research stems from several key factors; their cost-effective "bottom–up" fabrication and high-yield reproducible electronic properties [26-28], which pave way for some fabrication challenges, higher carrier mobility, smooth surfaces and the ability to produce radial and axial Nano-wire hetero-structures [29-30], better scalability resulting from the fact that diameter of Nano-wires can be controlled down to well below 10 nm [31-32]. However, due to their smaller diameters, the inversion charge changes from surface inversion to bulk inversion due to quantum confinement. Thus, variations in Nano-wire dimensions due to fabrication imperfections can lead to perturbations in the carrier potential and scattering that degrade the charge transport characteristics. Also, variations in Nano-wire diameters may lead to a variation in FET threshold voltage. Reducing variability is therefore a key challenge in making Nano-wire FETs a viable technology. Furthermore, quantum confinement effects make modeling of Nano-wire transistors a complex problem. The physics related to the operation of Nano-wire transistors needs to be well articulated so that simple compact models, including ballistic transport and realistic sub band parameters, can be developed for circuit design using SPICE-like simulators [33].

3. PROPOSED ARCHITECTURE

3.1 INTRODUCTION

There are two vigorously irrelevant approaches of two electrons in the QCA cell for an evacuated cell, expected cell polarization P=+1 and cell polarization P=-1.while Cell polarization P=+1 alludes to parallel 1 while cell polarization P=-1 alludes to relating 0.In expansion, this thought is graphically potrayed in figure - 1.It is additionally colossal that there is an unpolarized state as well. In an unpolarized state, potential points of confinement between contact are diminished which diminishes the exhibit generally zero polarization and the two electron wave limits have been delocalized over the telephones appeared in Figure 1

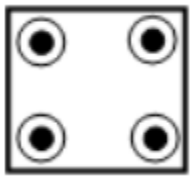


Fig 1.unpolarized cell

The numbering of specks signified by electrons in the cell goes clockwise beginning from the matrix on the upper appropriate with quantum level I =1, base right cell I =2, base left cell I =3,

International Journal For Recent Developments in Science & Technology
Crossref
A Peer Reviewed Research Journal
2581-4575

and upper left cell i=4. The polarization level P in a cell is characterized as Where Pi means the electronic charge at speck current. The polarization estimates the charge design for example the degree to which the electronic charge is appropriated among the four cells. The basic QCA sensible circuit is the three-input majority gate(MG) that shows up in Figure 2 from which progressively complex circuits can be fabricated. The fundamental MG gates are acquired by setting four neighboring cells bordering to a quantum cell, which is in the center. Three of the side cells are utilized as data sources, while the staying one is the yield. The quantum cell will consistently expect the majority polarization is where there will be at least charge between the electrons in the three information cells and the quantum cell.

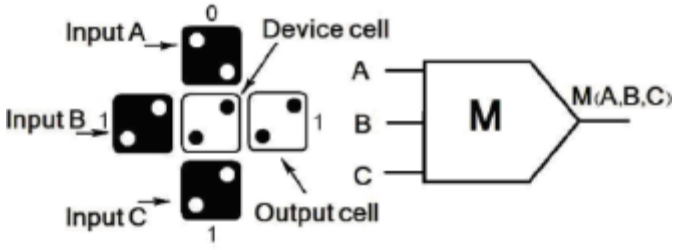


Fig 2.Majority gate using QCA

Consider the coulombic interface between cells 1 and 4,cells 2 and 4,cells 3 and 4 to perceive how the contraption cell accomplishes its most minimal imperativeness state (and from now on P=+1 in figure2).Typically, coulombic association between electrons in cells 1and 4 would make 4 change its polarization in light of electron stun. (expecting cell 1 is a data cell). In any case, cells 2 and 3 in like manner sway the polarization of cell 4 and have polarization P=+1. Along these lines, in light of the way that the greater part of the cells influencing the contraption cell have polarization 1 P , it additionally will moreover expect this polarization because the forces of Coulombic association are more grounded for it than for 1.

Fig. 4. Schematic of Existing Full Subtractor design

The schematic depiction of full subtractor circuit is appeared by Fig.4. The utilization of 5-input MGs make the circuit more straightforward than utilizing just 3-input MG and inverter from literature [2].

3.2. PROPOSED DESIGN:

The major drawback from the above literature is that they consumed the more area, thus they used the more power consumption. The number of majority gates they used to generate the full adder and subtractions are two 3-input Majority gates, two 5-input majority gates And also they required the four inverter gates. To optimize this the new design has been developed which is works both full adder and full subtractor at a time.

3.3 PROPOSED ADDERS AND SUBTRACTORS:

The proposed method is implemented with only three 3-input majority gates and two inverters and there is no need of five input majority gates. So the number of quantum cells will reduced in this design method, it causes to reduce the area as well as power.

International Journal For Recent Developments in Science & Technology
Crossref
A Peer Reviewed Research Journal
2581-4575

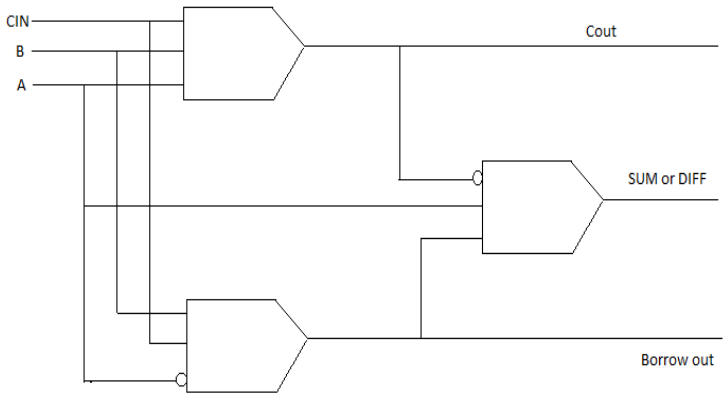


Fig. 3. Schematic of proposed Full adder and Subtractor

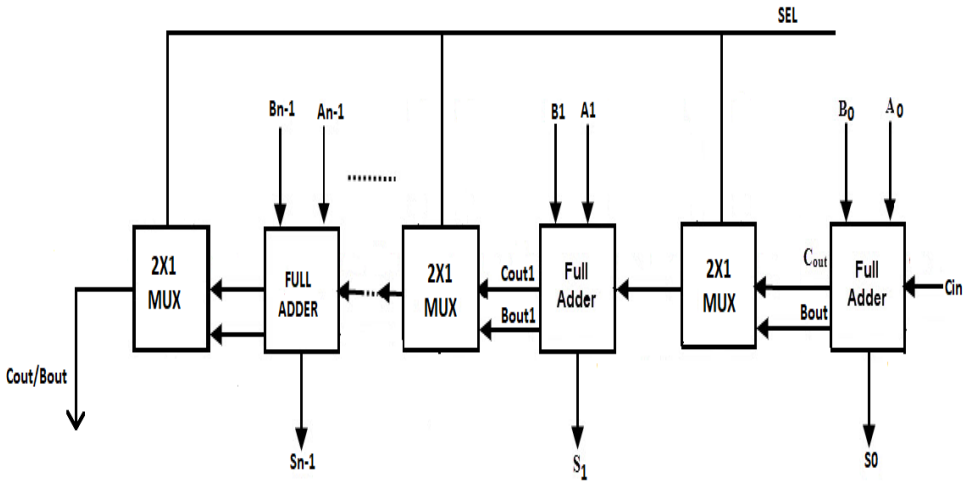


Fig. 4. Schematic of proposed N-bit adder and Subtractor

The above figure represents the Full adder and Subtractor, here the single circuit will performs the both operations. Majority gate M1 will generate the carry out and Majority gate M2 will generate the borrow out. Carry out and Borrow out as well as input A will be applied as inputs to the 3rd majority gate to generate the sum or diff.

The above figure represent the N-bit adder and Subtractor by connecting the series manner of N stages. The each FAFS block represents the fig 5 with the majority logics. Here, the carry out and borrow out of the first FAFS block will be applied as input to the next stage. If we required adder as the functionality then carry out will be applied as carry in by making the selection line of 2to1mux to zero, If we required subtractor as the functionality then borrow out will be applied as carry in by making the selection line of 2to1mux to one. The mux operation using majority gates will be explained in this paper in further chapters.

3.4 PROPOSED MULTIPLIERS

International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal

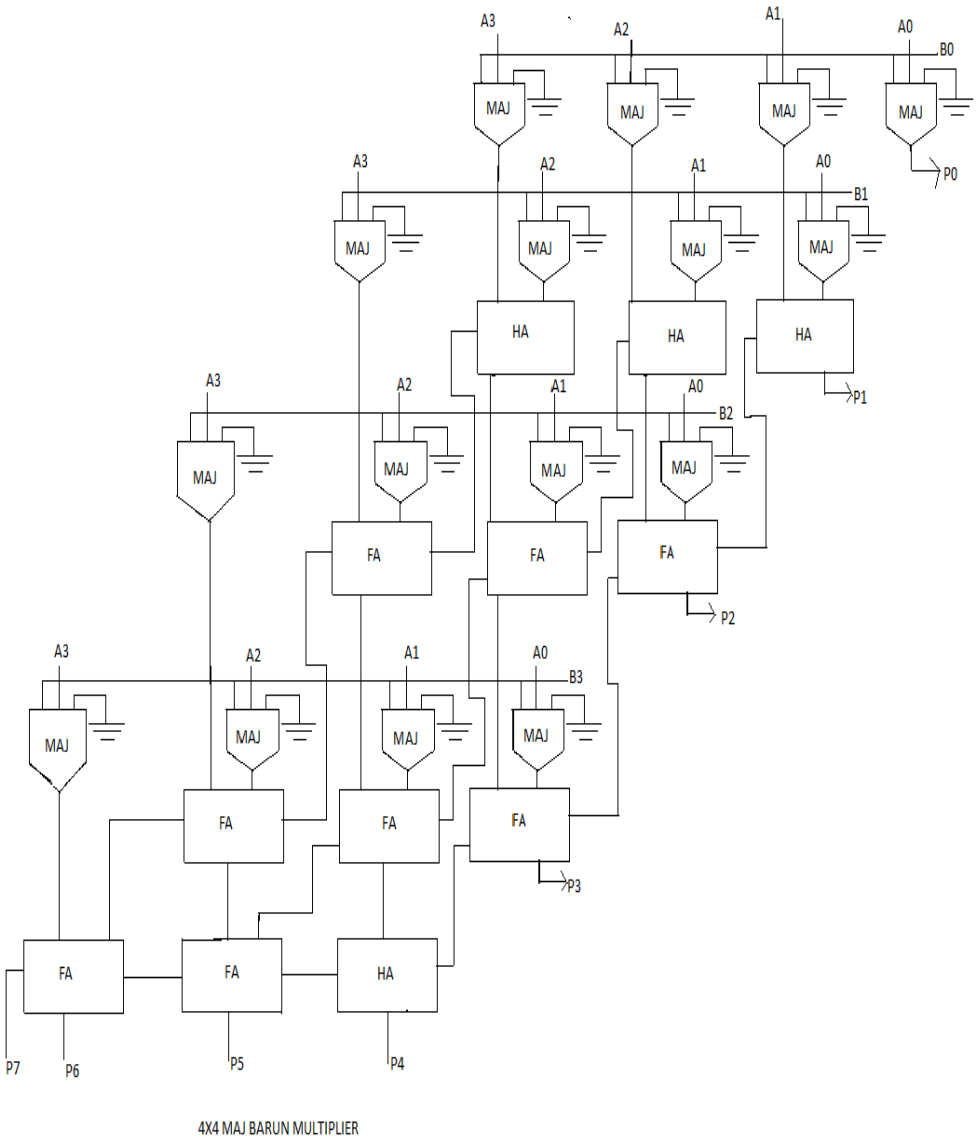


Fig. 5. Schematic of 4x4 Barun Multiplier

The above figure performs the 4 bit multiplication operation between A,B. Initially, 16 partial precuts namely A0B0, A1B0, A0B1 and so on generated by using bitwise Majority gates operation between A,B and ground. By making any one of the input zero in the majority gate it will act as the AND gate. For implementing the half adder, by making the anyone of the input in Full-adder zero and the Full adder circuit is represented in Fig 5.

International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal

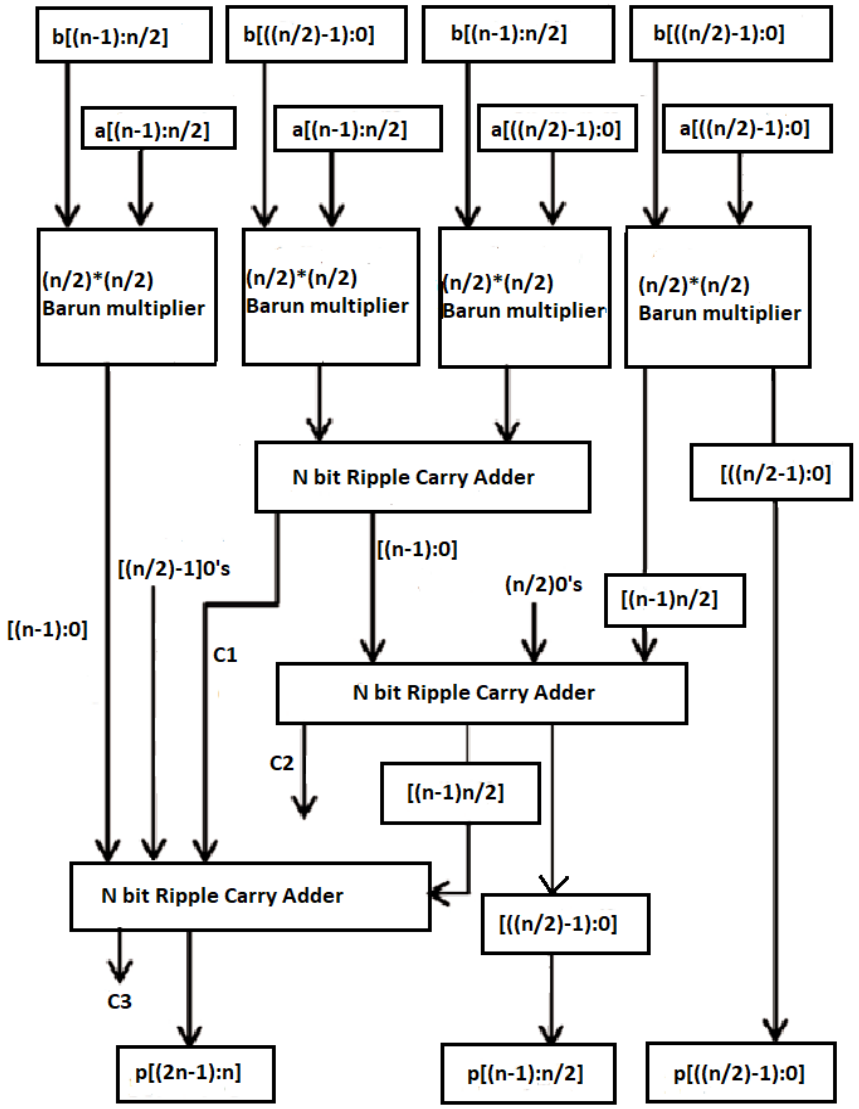


Figure 6 : Schematic diagram of N bit multiplier

For develop the N-bit multiplier, it needs 4 Nby2 multipliers. For example, for implementing 8 bit multiplier it requires four 4-bit baurn multipliers. Here, three N-bit Ripple carry adders are used as developed in fig. 6 in this paper. First adder adds the outputs of second and third multiplier partial products here, and addition output will forward to second stage adder. First Nby2 baurn multiplier half of the lsb output bits fed as the final outputs, next half msb output bits fed as the input to the second stage adder. in order to avoid the size of array mismatches Nby2 zeros added to second and third stage adders. After completing the all successful addition product P will generate.

3.4.1 LOGICAL UNIT

As part of the logical unit here we are considered either AND operations and OR operations. By making anyone of input zero in majority gate it will act as the AND gate and similarly by making anyone of input or in majority gate it will act as the OR gate. Inversions of AND, OR gate will

International Journal For Recent Developments in Science & Technology
Crossref
A Peer Reviewed Research Journal
2581-4575

create the universal gates like NAND and NOR gates. In the, The FAFS deisgn it has SD pin as three input XOR function, and inversion of it creates XNOR gate.

3.4.2 PROPOSED 4to1 MULTIPLEXER:

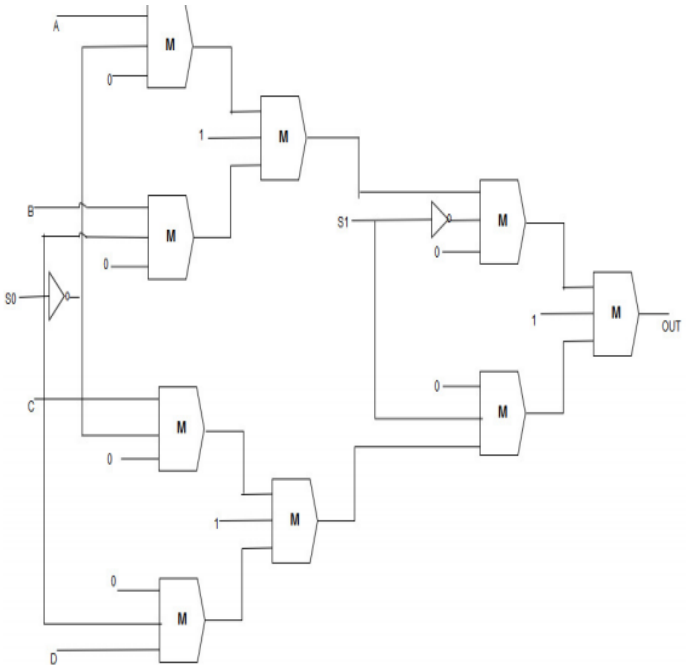


Figure 7: 4to1 multiplexer using QCA

A 4to1 Multiplexer can be implemented with by the series and parallel design of 2:1 multiplexer. The equation of 4:1 multiplexer can be derived as:

F=D.S0.S1+C.S0.S1B+ B.S0B.S1+ A.S0B.S1B.

Where S0, S1 represents the selection lines and A, B, C, D represents the 4to1 multiplexer inputs, S1B, SOB are compliments of S1 and S0. The MG gate representation of the 4:1 multiplexer is shown in Figure 9.

3.4.3 ALU:

International Journal For Recent Developments in Science & Technology
Crossref
A Peer Reviewed Research Journal
2581-4575

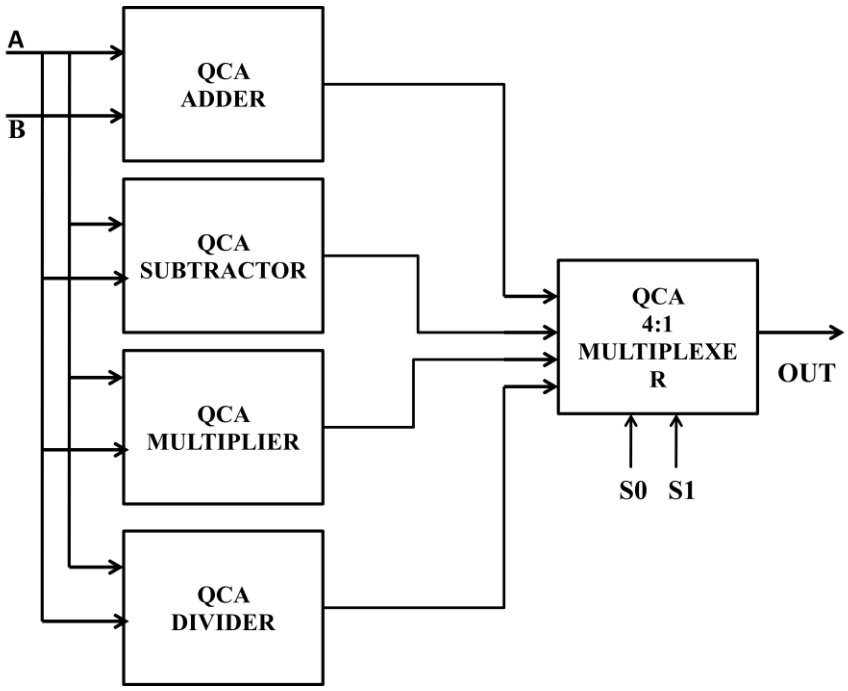
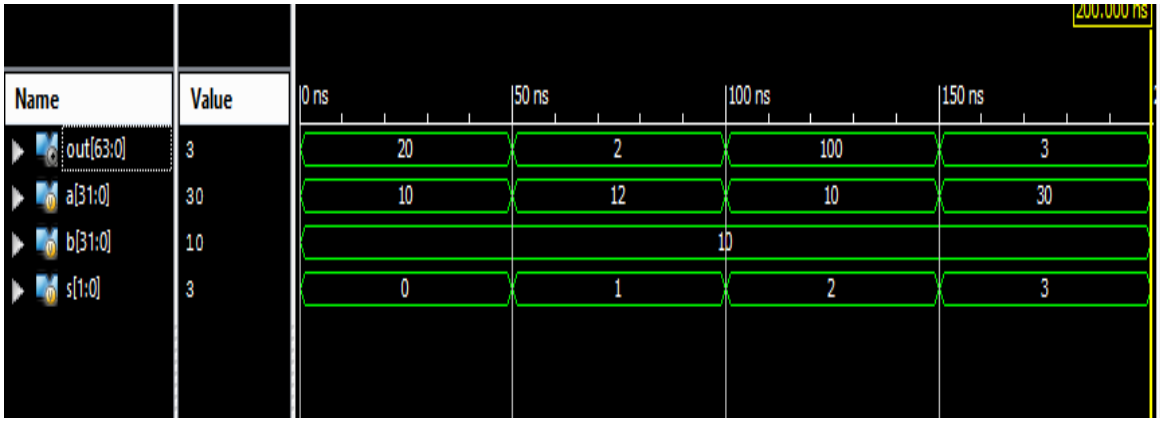


Figure 8: Block diagram of Nano-Caluculator

The proposed Nano-Caluculator performs four operations between inputs A and B. when multiplexer selection lines S0 and S1 becomes {0, 0}, it will functions as Adder, similarly for {0,1}functions as subtractor, for {1,0} functions as multiplier and for {1,1} act as logical unit.

4. SIMULATION RESULTS

4.1 WAVEFORMS



The above result represents the simulation waveform by using the Xilinx ISE software. Where S is the selection line, if s is 0 then a,b {10,10}added generates the output as 20, s is 1 then a,b {12,10}subtracted generates the output as 2, s is 2 then a,b {10,10}multiplied generates the output as 100 and s is 3 then a,b {30,10}logical unit generates the result as 3.

International Journal For Recent Developments in Science & Technology
Crossref
A Peer Reviewed Research Journal
2581-4575

4.2 DESIGN SUMMARY

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice LUTs	4982	204000	2%
Number of fully used LUT-FF pairs	0	4982	0%
Number of bonded IOBs	131	600	21%

The above result represents the synthesis implementation by using the Xilinx ISE software. From the above table, it is observed that only 4982 look up tables are used out of available204000. It indicates very less area(2%) was used for the proposed design.

4.3 TIME SUMMARY

```
LUT2:I0->O            1    0.043   0.000  div1/Madd_GND_49_o_GND_49_o_a
MUXCY:S->O            1    0.230   0.000  div1/Madd_GND_49_o_GND_49_o_a
XORCY:CI->O           2    0.251   0.347  div1/Madd_GND_49_o_GND_49_o_a
LUT4:I2->O            1    0.043   0.000  div1/Msub_n0258_Madd_lut<30>
MUXCY:S->O            0    0.230   0.000  div1/Msub_n0258_Madd_cy<30> (
XORCY:CI->O           1    0.251   0.289  div1/Msub_n0258_Madd_xor<31>
LUT5:I4->O            1    0.043   0.279  Mmux_out110 (out_0_OBUF)
OBUF:I->O                 0.000          out_0_OBUF (out<0>)
----------------------------------------
Total                     54.238ns (31.895ns logic, 22.343ns route)
                                   (58.8% logic, 41.2% route)
```

The above result represents the time consumed such as path delays by using the Xilinx ISE software.the consumed path delay is 54.238ns.

4.4 POWER SUMMARY

International Journal For Recent Developments in Science & Technology
Crossref
A Peer Reviewed Research Journal
2581-4575

Device			On-Chip	Power (W)	Used	Available	Utilization (%)		Supply Summary		Total	Dynamic	Quiescent
Family	Virtex7		Logic	0.000	3709	204000	2		Source	Voltage	Current (A)	Current (A)	Current (A)
Part	xc7vx330t		Signals	0.000	4570	---	---		Vccint	1.000	0.086	0.000	0.086
Package	ffg1157		IOs	0.000	131	600	22		Vccaux	1.800	0.030	0.000	0.030
Temp Grade	Commercial		Leakage	0.143					Vcco18	1.800	0.001	0.000	0.001
Process	Typical		Total	0.143					Vccbram	1.000	0.002	0.000	0.002
Speed Grade	-3												
			Thermal Properties		Effective TJA (C/W)	Max Ambient (C)	Junction Temp (C)				Total	Dynamic	Quiescent
Environment					1.4	84.8	25.2		Supply Power (W)		0.143	0.000	0.143
Ambient Temp (C)	25.0												
Use custom TJA?	No												
Custom TJA (C/W)	NA												
Airflow (LFM)	250												
Heat Sink	Medium Profile												
Custom TSA (C/W)	NA												
Board Selection	Medium (10"x10")												
# of Board Layers	12 to 15												
Custom TJB (C/W)	NA												

The above result represents the power consumed by using the Xilinx ISE software. The consumed power is 0.143uw.

COMPARASION TABLE

parameter	**EXISTING METHOD[1]**	**PROPOSED METHOD**
Time delay	59.110 ns	54.238 ns
Power utilized	1.293uw	0.143 uw
Look up tables	5277	4982

5.CONCLUSION

In this paper, a new QCA based N-bit adders, subtractions and multipliers designs has developed to perform the arithmetic and logical operations. The simulation outcome confirms the proposed operations have developed with less cells, area and latency. In addition, to decrease the complication of the addition associated operations, an proficient adder-subtractor has been proposed.

REFERENCES

[1] C. S. Lent, P. D. Tougaw, W. Porod, and G. H. Bernestein, "Quantum cellular automata," *Nanotechnology*, vol. 4, no. 1, pp. 49–57, 1993.

[2] M. T. Niemer and P. M. Kogge, "Problems in designing with QCAs Layout = Timing," *Int. J. Circuit Theory Appl.*, vol. 29, no. 1,pp. 49–62, 2001.

[3] J. Huang and F. Lombardi, *Design and Test of Digital Circuits by Quantum-Dot Cellular Automata*. Norwood, MA, USA: Artech House,2007.

[4] W. Liu, L. Lu, M. O'Neill, and E. E. Swartzlander, Jr., "Design rules for quantum-dot cellular automata," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2011, pp. 2361–2364. [5] K. Kim, K. Wu, and R. Karri, "Toward designing robust QCA architectures in the presence of sneak noise paths," in *Proc. IEEE Design, Autom. Test Eur. Conf. Exhibit.*, Mar. 2005, pp. 1214–1219.

[6] K. Kong, Y. Shang, and R. Lu, "An optimized majority logic synthesis methology for quantum-dot cellular automata," *IEEE Trans. Nanotechnology*.vol. 9, no. 2, pp. 170–183, Mar. 2010.

[7] K. Walus, G. A. Jullien, and V. S. Dimitrov, "Computer arithmetic structures for quantum cellular automata," in *Proc. Asilomar Conf.Sygnals, Syst. Comput.*, Nov. 2003, pp. 1435–1439.