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A Low-Power Timing-Error Controlling By Timing Error Tolerant Circuitwith Time Borrowing Technique

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ABSTRACT

Timing error is now getting increased attention due to the high rate of error-occurrence on semiconductors. Even slight external disturbance can threaten the timing marginbetween successive clocks since the latest semiconductor operateswith high frequency and small supply voltage. To deal with atiming error, many techniques have been introduced. Neverthe-less, existing methods that mitigate a timing error mostly havetime-delaying mechanisms and too complex operation, resulting in a timing problem on clock-based systems and hardware overhead .In this article, we propose an oveltiming-error-to lerant method that can correct a timing error in stantly through a simple mechanism. By modifying a clock in a flip-flop, the proposed system can recover a timing error without the loss of time in the clock-based system. Further more, due to the compact mechanism, the proposed system has low hardware overhead incomparison with existing timing-error-tolerant systems that canrecover the error instantly. To verify our method, the proposedcircuit was extensively simulated by addressing PVT variations. Moreover, it was implemented in several benchmark designs, including a microprocessor.

Index Terms: Error detectionandcorrection,fault-tolerantsystems,softerror,timing-error-tolerantsystem,timingerror.

INTRODUCTION

Timing errors are an increasing reliability concern in nanometer technology, high complexity and multi-voltage\frequency integrated circuits. A local error detection and correction technique is presented in this work that is based on a new bit flipping flip-flop. Whenever a timing error is detected, it is corrected by complementing the output of the corresponding flip-flop. The timing-error rate is increased as the clock frequency is increased. Since the clock period is getting minimized, critical paths in the circuit are

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susceptible to timing errors. Furthermore, variations on the CMOS process, power supply, and temperature impact the performance of modern integrated circuits, which results in the high incidence of timing errors. As the supply voltage decreases, the delay of the circuit can drastically change between the typical case and the worst case of process, voltage, and temperature (PVT) conditions. Process variability in device and circuit parameters is one of the primary challenges currently faced by the semiconductor industry.

Moreover, transistor aging issues are critical for the occurrence of timing errors. Due to the negative-bias temperature instability (NBTI) in CMOS, the threshold voltage is lowered, which finally increases the path delays of logics. Hence, a timing-error-tolerant method is highly required in order to implement reliable systems. Error tolerance refers to the ability of a system to function even after an error has occurred. In other words, an error tolerant system is one in which the results of making errors are relatively harmless. Besides static variations that occur during chip fabrication, dynamic parameter variation – resulting from environmental and workload changes – is also possible during the chip's operation. Examples of dynamic variations include supply voltage droops, temperature changes, and transistor aging degradation. Variations change the circuit's characteristics in terms of timing and power consumption, and, thus, if not appropriately handled, they may adversely impact performance, power, and the system's overall reliability.

LITERATURE REVIEWS

M. Seok, G. Chen, S. Hanson, M. Wieckowski, D. Blaauw and D. Sylvester, "CAS-FEST 2010: Mitigating Variability in Near-Threshold Computing," in IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 1, no. 1, pp. 42-49, March 2011.

Near threshold computing has recently gained significant interest due to its potential to address the prohibitive increase of power consumption in a wide spectrum of modern VLSI circuits. This tutorial paper starts by reviewing the benefits and challenges of near threshold computing. We focus on the challenge of variability and discuss circuit and architecture solutions tailored to three different circuit fabrics: logic, memory, and clock distribution. Soft-edge clocking, body-biasing, mismatch-tolerant memories, asynchronous operation and low-skew clock networks are presented to mitigate variability in the near

threshold V_{DD} regime.

Summary: Due to the negative-bias temperature instability (NBTI) in CMOS, the threshold voltage is lowered, which finally increases the path delays of logics is studied.

M. Agarwal, B. C. Paul, M. Zhang and S. Mitra, "Circuit Failure Prediction and Its Application to Transistor Aging," 25th IEEE VLSI Test Symposium (VTS'07), 2007, pp. 277-286.

Circuit failure prediction predicts the occurrence of a circuit failure before errors actually appear in system data and states. This is in contrast to classical error detection where a failure is detected after errors appear in system data and states. Circuit failure prediction is performed during system operation by analyzing the data collected by sensors inserted at various locations inside a chip. We demonstrate this concept of circuit failure prediction for a dominant PMOS aging mechanism induced by negative bias temperature instability (NBTI). NBTI-induced PMOS aging slows down PMOS transistors over time. As a result, the speed of a chip can significantly degrade over time and can result in delay faults. The traditional practice is to incorporate worst-case speed margins to prevent delay faults during system operation due to NBTI aging. A new sensor design integrated inside a flip-flop enables efficient circuit failure prediction at a low cost. Simulation results using 90nm and 65nm technologies demonstrate that this technique can significantly improve system performance by enabling close to best-case design instead of traditional worst-case design.

Summary: In this paper, we have analyzed how the transistor aging effects the timing errors.

EXISTING METHOD

The time borrowing is a well-known concept in pipelines designed with pulsed latches or soft-edge flip-flops where valid signal transition is allowed even after the clock edge (during the limited transparent time period) resulting in propagation of correct values to the next stage. The optimization of transparency windows of pulsed latches can achieve the minimum power-delay product of pipelines. This approach uses a special latch, hereafter, referred to as the pulsed latch with time-borrowing detection (LTD), only at the timing critical paths of all pipeline stages. The LTD operates as a pulsed latch where the pulse width defines the time-borrowing window. The occurrence of the critical-path transition within is defined as a time-borrowing event. The LTD allows time

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borrowing in the current stage and generates a detection signal when critical paths are activated.

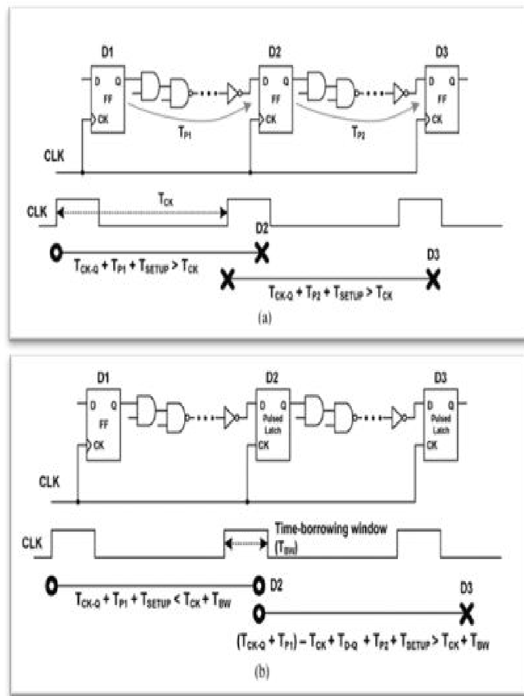

Fig.1: The conceptual operation of the pipeline with (a) the flip-flops, (b) the pulsed latches

DISADVANTAGES

While the system can avoid the penalty of the clock, it requires a large amount of hardware, such as an additional flip-flop and latch. Furthermore, since the location of the halfway of the combinational circuits is inaccurate and it is hard to be chosen, the transparent window can be made erroneously.

PRAPOSAL METHOD

we propose a timing-error-tolerant method that can correct a timing error immediately through a simple mechanism. In the critical path, the abnormal data transition after the rising edge of the clock, which is caused by a timing error, is detected and corrected by controlling the transparent window of the clock. The timing error is corrected directly through a minimum number of logics. Furthermore, our time-borrowing method that copes with the successive errors is introduced. If the timing error occurs in two stages successively, modified CLK in the second stage maintains a transparent window for enough time to make normal data be stored without changing system CLK.

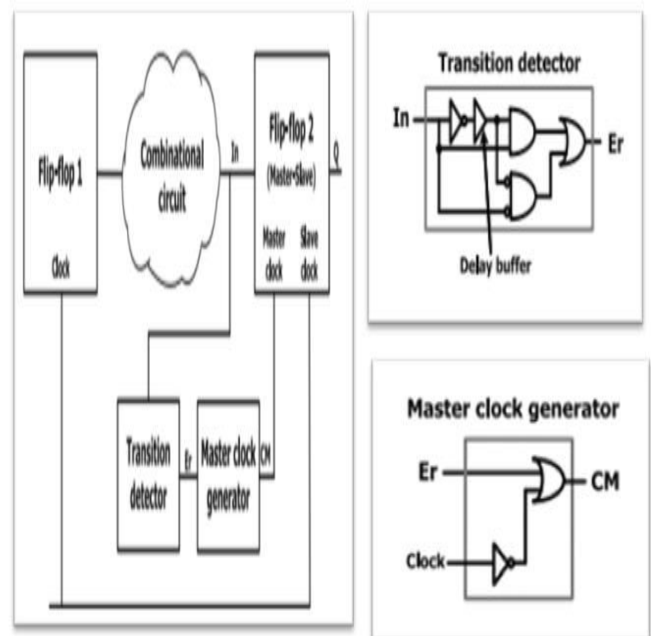

Fig.2: Timing error tolerant circuit diagram

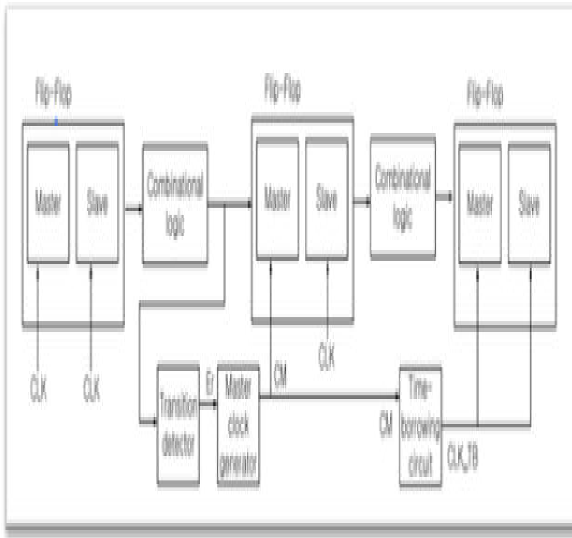

Fig.3: Timing error tolerant circuit using time borrow technique

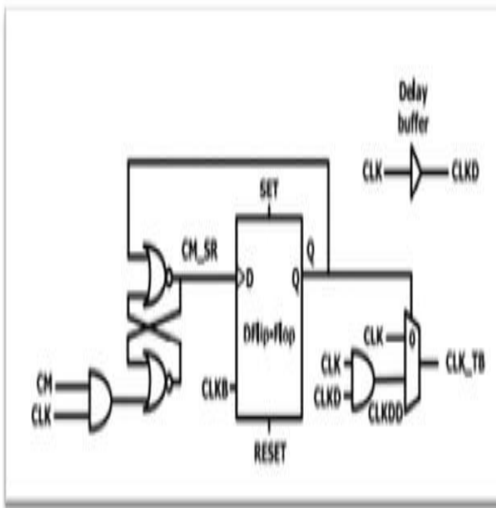

Fig.4: Time borrow circuit

ADVANTAGES

1. No need of additional clock for error recovery due to controlling action of clock signal.
2. Error detects and corrects instantly.
3. Low Area overhead as it consists of less no. of logics.
4. Avoid of clock penalty for time borrower circuit.

STIMULATION RESULT

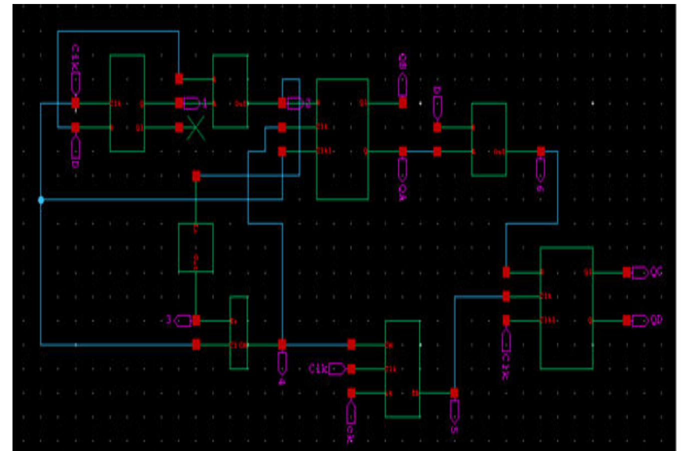

Fig.5: Schematic diagram of proposed system using time borrow Technique

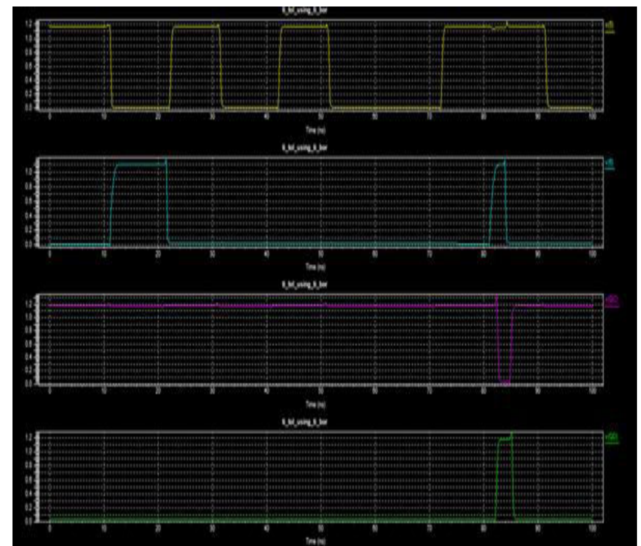

Fig.6: Waveforms for timing error tolerant circuit using time borrow technique

Using the information acquired from the timing analyzingtool, the critical paths of the circuit and the setup-time infor-mationofeachelementinthecircuitaredetermined.Wemakefull use of such results to

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choose the best location for ourproposed system. If a single-stage error occurs, the delayedarriving data signal is recovered because the master latch istransparentforthepulseperiod.However,if asuccessive-stageerror occurs due to the lack of setup time in the second-stageflip-flop, the delayed arriving data signal in the second stagecannot be stored because of the setup-time violation. To dealwiththesuccessive-stageerror,wedevisedthetime-borrowingtechnique. The time-borrowing circuit is provided in the secondstage

Comparison of existing method and proposed method output specifications

Existing method theroticalvalues :-

1. Delay = 8.2001e-008 sec
2. Average power = 6.91169e-006 watts
3.Area = 219

Delay Proposed method praticalvalues :-

Without time borrowing :-

1.Delay = 1.4296e-008
2.Average power = 6.010679e-004 watts
3.Area = 106

withtimeborrowing:-

1. Delay = 7.2247e-008
2. Average power =1.552405e-003 watts
3.Area = 216

CONCLUSION

In this article, we propose a timing-error-tolerant method that can correct a timing error immediately with a compact circuit structure. We have presented an effective method to detect and correct timing errors using Timing error tolerant circuit and Tolerant circuit using Time borrowing technique. In the critical path, the abnormal data transition after the edge of the clock can be detected and corrected by controlling the transparent window of the clock. The timing error is corrected directly through a minimum number of logics. Furthermore, our time-borrowing technique that deals with the successive-stage error is introduced. If the timing error occurs in the second stage successively, modified CLK maintains the transparent window during enough period of time for timing-error tolerance without changing system CLK.

Our proposed system is designed to operate the targeted function, but it is not yet designed with consideration for possible glitches. Since the glitch occurs for a short duration, the glitch can be removed by adjusting CMOS parameters. For instance, if the width or the length of transistors in the "transition detector" is changed, the glitch can be removed by adjusting the rising or falling slope. With this technique, signal "Er" could be delayed, which can result in a little lower performance. On the other way, the glitch

can be removed by changing the circuit of the "transition detector," which could cause larger hardware overhead. To address the glitch, we can adopt one of the methods that are stated above in further study.

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