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LOW POWER HIGH ACCURACY APPROXIMATES MULTIPLIER USING APPROXIMATE HIGH ORDER COMPRESSORS

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ABSTRACT

This project presents the design of approximate 15-4 compressor using 5-3 compressors as basic module. Four different types of approximate 5-3 compressors are used in a 15-4 compressor for less power consumption and high pass rate. We have analysed the results in all the cases. A 16 bit multiplier is simulated using the proposed 15-4 compressor. Simulation results show that the multipliers with proposed approximate compressors achieve significant improvement in power as compared to the multipliers with accurate 15-4 compressor. Pass rate of the proposed multipliers are high as compared to other existing approximate multipliers. Finally, the proposed multiplier is used in image processing applications where the peak signal to noise ratio (PSNR) of the image is measured. Quality of the image is compared with an accurate multiplier and the obtained results show that our proposed multiplier performs better than existing approximate multiplier.

Keywords: Compressor, DSP, MED, NED, ED, XOR, XNOR.

I.INTRODUCTION

MOST Computer Arithmetic Applications Are Implemented Using Digital Logic Circuits, Thus Operating With A High Degree Of Reliability And Precision. However, Many Applications such as in multimedia and image processing can tolerate errors and imprecision in computation and still produce meaningful and useful results. Accurate and precise models and algorithms are not always suitable or efficient for use in these applications. The paradigm of inexact computation relies on relaxing fully precise and completely deterministic building modules when, for example, designing energy-efficient systems. This allows imprecise computation to redirect the existing design process of digital circuits and systems by taking advantage of a decrease in complexity and cost with possibly a potential increase in performance and power efficiency. Approximate (or inexact) computing relies on using this property to design simplified, yet approximate circuits operating at higher performance and/or lower power consumption compared with precise (exact) logic circuits. Addition and multiplication are widely used operations in computer arithmetic; for addition full-adder cells have been extensively analyzed for approximate computing Liang et al. has compared these adders and proposed several new metrics for evaluating approximate and probabilistic adders with respect to unified figures of merit for design assessment for inexact computing applications. For each input to a circuit, the error distance (ED) is Defined as the arithmetic distance between an

erroneous output and the correct one. The mean error distance (MED) and normalized error distance (NED) are proposed by considering the averaging effect of multiple inputs and the normalization of multiple-bit adders. The NED is nearly invariant with the size of an implementation and is therefore useful in the reliability assessment of a Specific design. The tradeoff between precision and power has also been quantitatively evaluated. However, the design of approximate multipliers has received less attention.

Multiplication can be thought as the repeated sum of partial products; however, the straightforward application of approximate adders when designing an approximate multiplier is not viable, because it would be very inefficient in terms of precision, hardware complexity and other performance metrics. Most of these designs use a truncated multiplication method; they estimate the least significant columns of the partial products as a constant. In an imprecise array multiplier is used for neural network applications by omitting some of the least significant bits in the partial products (and thus removing some adders in the array). A truncated multiplier with a correction constant is proposed. Microprocessors and Digital Signal Processors(DSP) are playing a significant role to handle thecomplexity of digital signal. About 95% of the processorsin the market are based on digital signal [1]. Digital signal processors take care of convolution, correlation and filtering of digital signal [2]. Multipliers, shifters and adders are mainly used to accomplish these tasks. Among the three modules, multiplier is the most complex one. Multipliers take more time and consume higher power than other two modules [3]. Multipliers have three phases - generation of partial

Products, reduction of partial products and final stage addition. Reduction of partial products take much time and power inthe multiplier. Many techniques were proposed to reduce the critical path in the multiplier [4]-[5]. Among them, the use of compressors in partial product reduction stage is the most popular. Compressors are basic circuits which are made of full adders or half adders to count the number of “ones” in the input. Several compressors are required in the partial product reduction stage. Various compressors such as 3-2, 4-2, 5-2 And 5-3 were proposed by researchers in the last 20 years [6]-[9].These are useful only when the size of multiplier is small. 16 _ 16, 32 _ 32 bit multipliers require large size of compressors. High order compressors provide better results interns of power and speed [10]-[12]. But it consumes morearea than low order compressors. All these techniques perform the exact computation and modulesproduce the correct result. Accuracy of the module/device is always 100% in exact computing. But exact computing has one major drawback. It is not possible to optimize all the parameters of the circuit in exact computing. However, exact computing is not essential for every application. There are some applications like image processing and multimedia can tolerate errors and provide meaningful results. Inexact (approximate) computing techniques have become popular because of its low complexity and less power consumption. Inexact computing produces reasonable result, even it has low accuracy. In approximate computing, the value of error rate (ER), error distance (ED) and normalized error distance (NED) play an

important role to calculate the final output [13]. Error rate is given by a number of erroneous outputs over the total number of outputs. Error Distance is the arithmetic distance between an erroneous output and the correct one. Normalized Error Distance is the ratio of mean error distance over all inputs by maximum input of the circuit. Several approximation techniques were proposed for adders and multipliers [14]-[32].From central point to the most significant bit (MSB) is called accurate and to the least significant bit (LSB) is called inaccurate part of adders which was discussed by Ning Zhun et al [14]. Inaccurate computing in MSB side causes large error. The normal addition rule is applied in accurate part whereas a special method of addition takes place in inaccurate part.Output "sum" value is calculated normally when any one of the operand value of adder is "0". When both operands are"1", "sum" value can be fixed as "1" from that bit positionto least significant bit. This technique is used to minimize the error distance of the adder.

Approximate XOR/XNOR adder for inexact computing isproposed by Zhixi Yang et al in [15]. Both XOR and XNOR gates are required to calculate the output of the adder. Three different approximate methods were proposed. The output expression for "sum" and "carry" is approximated. Instead of using two XOR gates, only one XNOR gate has been utilized to calculate "sum". Similarly, one XOR, one OR and two AND gates are used for "carry". Low power imprecise adder were proposed by Honglan Jiang et al in [16] where they optimized transistor count, power consumption and power delay product (PDP) of the adder. Moreover, the number of incorrect outputs of the adder is also small. In [7]-[8], accuracy, error distance and various design parameters of approximate adders are analysed and compared. Approximation methodologies were applied in generating the partial product phase [9]. A 2 _ 2 bit approximate multiplier is designed by altering the one output combination. In this technique, multiplier produces "7d" when it multiplies "11" by "11". But the actual output of the multiplier is "1001". The probability of getting error in this multiplier is 0.0625. An error has been introduced in the partial product generation phase. Adder tree (reduction tree) of this multiplier is same as accurate multiplier. Several other approximation Several other approximation techniques were proposed in the partial product reduction stage. One need not consider the particular row of partial products when the value of multiplier bit is "0" also particular column value can be skipped when multiplicand bit is "0". This technique is called row and column bypassing. In [12], some of carry-save adders are skipped in both horizontal and vertical directions based on the number of zeros in the multiplier input. In [23], partial product tree is splitted into two parts. Accurate multiplier was used in MSB side of the multiplier. No multipliers was used in LSB side where approximation rule was applied.

II. LITERATURE SURVEY

[1] "Low Power High Accuracy Approximate Multiplier Using Approximate High-Order Compressors" by R. K. Gupta and S. J. S. R. Pillai (2017): This paper presents a novel approach to designing low-power, high-accuracy approximate multipliers by utilizing high-order compressors. The authors propose a method where approximations are introduced in the multiplication process, significantly

reducing the hardware complexity and power consumption without sacrificing much in terms of accuracy. The high-order compressors are used to approximate the multiplication results, with careful control of the approximation error to balance power efficiency and accuracy. Simulation results show that the proposed multiplier achieves substantial power savings compared to traditional multipliers while maintaining acceptable accuracy levels for many signal processing applications. This work is relevant for energy-efficient applications like image processing and machine learning.

[2] "Approximate Multiplication Using Compressors for Low Power Applications" by M. A. Alam and P. P. J. P. Kumar (2018): This paper focuses on the development of approximate multipliers based on high-order compressors for low-power applications. The authors introduce a new method for approximating the product of two numbers, wherein the multiplication is performed using a set of compressors that reduce the computational complexity. The approximations are designed to minimize error while significantly lowering the power consumption. The paper also discusses how the error in the multiplication operation can be controlled through the strategic selection of compressor configurations. The results indicate that this approach can be particularly useful for applications where power consumption is a critical factor, such as embedded systems and mobile devices.

[3] "Design of Low Power Approximate Multiplier for DSP Applications Using High Order Compressors" by S. T. Srinivasan and R. S. Subramani (2016): This paper presents a design of low-power approximate multipliers specifically for digital signal processing (DSP) applications, employing high-order compressors to reduce power consumption. The authors explore the trade-off between computational accuracy and power efficiency, showing that approximate multipliers can achieve significant power savings without a substantial loss in performance. High-order compressors are utilized to minimize the hardware resources required for multiplication while maintaining a reasonable level of approximation error. The proposed design is evaluated in the context of DSP applications, where the requirement for real-time performance often allows for some level of error in the computations. Simulation results demonstrate that the proposed method is well-suited for low-power DSP systems.

[4] "Energy-Efficient Approximate Multiplier Using High-Order Compressors for Multimedia Applications" by V. K. S. V. R. K. Naidu and K. S. R. Anjaneyulu (2020): This research paper investigates the use of high-order compressors in designing an energy-efficient approximate multiplier for multimedia applications. The authors propose an approach where the conventional exact multiplier is replaced by an approximate multiplier, which uses compressors to reduce power consumption while maintaining an acceptable level of accuracy. High-order compressors are employed to reduce the size of the intermediate products generated during multiplication. The accuracy of the approximation is fine-tuned to suit the specific requirements of multimedia applications, where some errors are tolerable in exchange for lower power consumption. Experimental results confirm that the proposed multiplier offers significant power savings, making it ideal for portable multimedia devices like smartphones and tablets.

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[5] "Approximate Multiplication with High-Order Compressors for Low Power and High-Speed Applications" by R. P. S. Reddy and N. R. Lakshmi (2019): This paper explores the design of approximate multipliers that utilize high-order compressors to achieve low power consumption while ensuring high-speed performance. The authors focus on applications where high-speed computation is critical, and some accuracy loss is acceptable. By incorporating high-order compressors into the multiplication process, the design reduces the need for extensive hardware resources and lowers power consumption significantly. The paper discusses various trade-offs between speed, power efficiency, and accuracy, demonstrating that the proposed method can be used in high-performance computing environments like digital communications and high-speed data processing. The results show that the approach provides a good balance between these competing factors, making it a promising solution for modern low-power, high-speed applications.

III.PROPOSED WORKING

This section describes the design of 15-4 compressor using approximate 5-3 compressors. The 15-4 compressor was proposed in [12] as shown in figure 4. This compressor has fifteen inputs (X0 - X14) and it produces four outputs (O0 - O3). This compressor has five full adders at first stage, two 5-3 compressors in second stage and final stage has parallel adder. Each full adder receives three primary inputs and it generates "Sum" and "Carry". "Sum" of all full adders is given to the 5-3 compressor. Similarly, "Carry" of all full adders is given to another 5-3 compressor. Outputs of the 5-3 compressors are given to the parallel adder. Parallel adder is used to generate the final output. In approximate 15-4 compressor, instead of using accurate 5-3 compressors, we have used proposed approximate 5-3 compressors. Full adders and parallel adders are kept as original adders in proposed 15-4 compressor.

Four approximate designs of 15-4 compressor are proposed. 5-3 compressors are used in first three designs of approximate 15-4 compressor which uses the design 1, 2 and 3 of proposed approximate 5-3 compressor. Design 1 and design 4 of proposed approximate 5-3 compressor are used in design 4 of 15-4 compressor. Design 1 approximate 5-3 compressor is used to handle "carry" signals because output "carry" has more weightage than "sum". Moreover, a pass rate of design 1 compressor is higher than design 4. Design 4 approximate 5-3 compressor is used to handle sum signals.

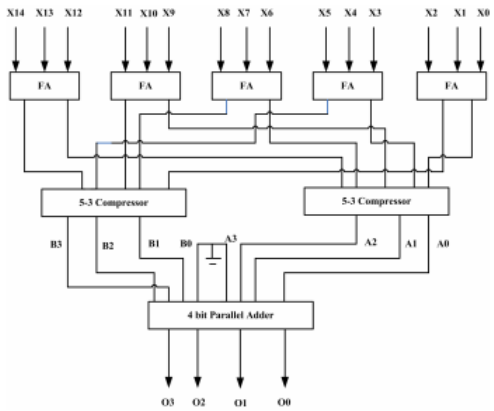

Fig.1. Proposed model.

The design of 16 × 16 multiplier is presented. Four approximate multipliers are designed using the proposed four 15-4 compressors. In addition to this, one accurate multiplier and four other approximate multipliers are considered. Approximate multipliers using the proposed approximate 15-4 compressors are compared with the accurate 16 × 16 multipliers with accurate 15-4 compressors

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and also with other multipliers designed using various other approximate compressors. Figure 5 shows the design of 16 × 16 bit multiplier using 15-4 compressor where, each dot represents one partial product. Six 15-4 compressors are used to design one multiplier in the partial product reduction and finally four multipliers are designed.

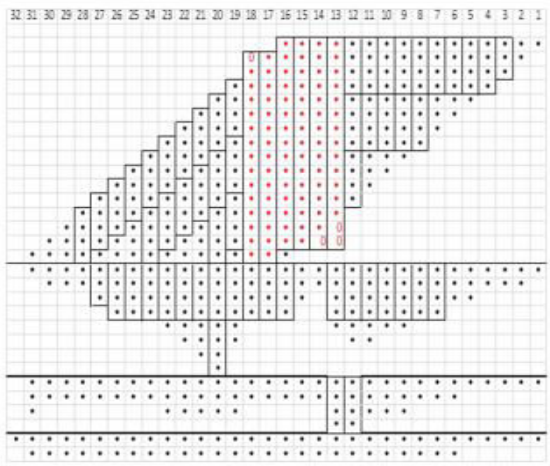

Fig.2. 16X16 model digram.

In figure, rectangular boxes indicate the use of 15-4 and 4-2 compressor in the multiplier. 15-4 compressors are used in the multiplier from 13th column onwards. Column number 13 of the multiplier has only thirteen partial products.

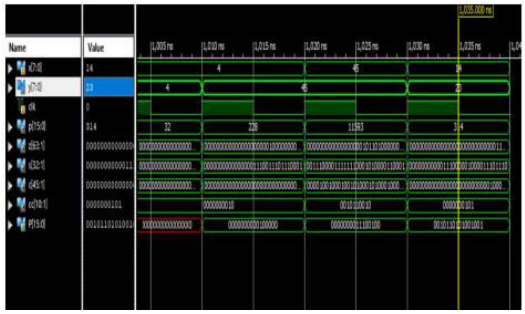

Fig.3. Output simulation results.

Two zeros are added in that column to make use of the 15-4 compressor. Similarly, one "0" is added in 14th column. Along with 15-4 compressors in the multiplier other accurate compressor like 4-2 and half, full adders are used for partial product reduction. Approximate compressors are used in 13th , 14th and 15th column of multipliers. Use of approximate compressors in most significant part would produce a larger error rate. Design 1 of 15-4 approximate compressor is used in multiplier 1. Similarly, design 2, 3 and 4 of 15-4 approximate compressors are used in multiplier 2, 3 and 4 respectively. In accurate multiplier, all accurate 15-4 compressors are used along with accurate 3-2 and 4-2 compressors.

Accurate 4-2 compressors, half and full adders are used in second and third stage of partial product reduction tree. In final stage, parallel adders are used to compute the final result.

IV.CONCLUSION

This paper presents the four designs of approximate 15-4 compressor. Approximate 16 × 16 bit multipliers are designed using those proposed 15-4 compressors. Approximate multipliers provide better performance than accurate multipliers with compromising of error rate. Moreover, we have achieved high pass rate and the normalized error distance value of multipliers designed using proposed 15-4 compressor is very small. Latency of the proposed multiplier is almost equal as compared to the accurate multipliers. In order to validate our work, image contrast has been performed with the help of proposed multiplier. The quality of the processed image shows that our proposed multipliers are working fine. The PSNR value of other approximate multiplier is less than 10 dB, but our proposed multiplier

IV.REFERENCES

[1] D. Liu Embedded DSP Processor Design, 1st ed.Morgan Kaufmann Publishing, 2008.

[2] K. K Parhi VLSI Digital Signal Processing Systems:Design and

Implementation., 1st ed.John Wiley and Sons, 1999.

[3] Y.Kim, Y.Zhang, and P. Li, "An energy efficient approximate adder with carry skip for error resilient neuromorphic VLSI systems," in proc. of International conference on Computer-Aided Design (ICCAD), Nov. 2013, pp. 130-137.

[4] A. Pishvaie, G. Jaberipur, and A. Jahanian, "Improved CMOS (4; 2) compressor designs for parallel multipliers," Computers and Electrical Engineering, vol. 38, no. 6, pp. 17031716, Nov. 2012.

[5] D. Baran, M. Aktan, and V.G. Oklobdzija V.G, "Energy Efficient Implementation of Parallel CMOS Multipliers with Improved Compressors," in proc. ACM/IEEE International Symposium on Low-Power Electronics and Design (ISLPED), Aug. 2010, pp. 147-152.

[6] S. Veeramachaneni, K. Krishna M, L. Avinash, S. R. Puppala, and M.B. Srinivas, "Novel Architectures for High-Speed and Low-Power 3-2, 4- 2 and 5-2 Compressors," in proc. of International Conference on VLSI Design (VLSID), Jan. 2007, pp. 324-329.

[7] R. Menon, and D. Radhakrishnan, "High performance 5: 2 compressor architectures," in proc. of IEE - Circuits, Devices and Systems, vol. 153, no. 5, Oct. 2006, pp. 447-452.

[8] A. Pishvaie, G. Jaberipur, and A. Jahanian, "High Performance CMOS (4:2) compressors," International journal of electronics, vol. 101, no. 11, pp. 1511-1525 Jan. 2014.

[9] O. Kwan, K. Nawka, and E. Swartzlander Jr, " A 16 bit by 16 bit MAC Design Using Fast 5:3 Compressor Cells," Journal of VLSI Signal Processing, vol. 31, no. 2, pp. 77-89, July 2002.

[10] S. Mehrabi, R.F Mirzaee, S. Zamanzadeh, K. Navi, and O. Hashemipour, "Design, analysis, and implementation of partial product reduction phase by using wide m:3 (4 m 10) compressors," Int. Journal of High Performance System Arch, vol. 4, no. 4, pp. 231-241, Jan. 2013.

[11] A. Dandapat, P.Bose, S. Ghosh, P Sarkar, and D. Mukhopadhyay, "A 1.2-ns 16 x 16 bit binary multiplier using high speed compressors," World Academy of Science, Engineering and Technology, vol. 39, pp. 627-632, March 2009.

[12] R. Marimuthu, M. Pradeepkumar, D. Bansal, S. Balamurugan, and P.S Mallick, "Design of high speed and low power 15-4 compressor," in proc. International Conference on Communication and Signal Processing (ICCSP), Apr. 2013, pp. 533-536.

[13] J. Liang, J. Han,and F. Lombardi, New metrics for the reliability of approximate and probabilistic adders," IEEE Trans. on Computers, vol. 63, no. 9, pp. 1760 - 1771, Sep.2013.

[14] N.Zhu, W L Goh, and Kiat Seng Yeo, "An enhanced low power highspeed adder for error tolerant application," in proc. of 12 th International Symposium on Integrated Circuits (ISIC), Nov. 2009, pp. 69 - 72.

[15] Z. Yang, A. Jain, J. Liang, J. Han, and F. Lombardi, "Approximate XOR/XNOR-based adders for inexact computing," in proc. of IEEE International Conference on Nanotechnology (IEEE - NANO), Aug. 2013, pp. 690 - 693.

[16] H. Jiang, J.Han, and F. Lombardi, "A comparative review and evaluation of approximate adders," in proc. of ACM Great Lakes Symposium on VLSI(GLSVLSI), May. 2015, pp. 343 - 348.

[17] V. Gupta, D. Mohapatra, S. P. Park, A. Raghunathan, and K. Roy, ”IMPACT: IMPrecise adders for low-power approximate computing,” in proc. of International Symposium on Low Power Electronics and Design (ISLPED), Aug. 2011, pp. 409 - 414.

[18] C. Liu, J. Han, and F. Lombardi, ”A Low-Power, High-Performance Approximate Multiplier with Configurable Partial Error Recovery,” in proc. of International Conference on Design Automation and Test in Europe (TEST), Mar. 2014.

[19] P. Kulkarni, P. Gupta, and M. D. Ercegovac, ”Trading accuracy for power in a multiplier architecture,” in Journal of Low Power Electronics, vol. 7, no. 4, pp. 490501, Dec. 2011.

[20] S. Balamurugan,and P.S Mallick, ”Fixed-width multiplier circuits using column bypassing and decompositon logic techniques,” in International journal on Electrical Engineering and Informatics, vol. 7, no. 4, pp. 655664, Dec. 2015.

[21] S. Balamurugan,S. Ghosh,Atul, S. Balakumaran, R. Marimuthu,and P.S Mallick, ”Design of low power fixed-width multiplier with row bypassing,” in IEICE Electronics Express, vol. 9, no. 20, pp. 15681575, Oct. 2012.

[22] H.R. Mahdiani, A. Ahmadi, S.M. Fakhraie, and C. Lucas, ”Bio-Inspired imprecise computational blocks for efficient VLSI implementation of softcomputing applications,” in IEEE Transactions on Circuits and Systems, vol. 57, no. 4, pp. 655664, Apr. 2010.

[23] K.Y. Kyaw, W.L. Goh, and K.S. Yeo, ”Low-power high-speed multiplier for error-tolerant application,” in proc. of IEEE International Conference of Electron Devices and Solid-State Circuits (EDSSC), Dec. 2010, pp. 1 - 4.

[24] K. Bhardwaj, P.S. Mane, and J. Henkel, ”Power- and area-efficient Approximate Wallace Tree Multiplier for error resilient systems,” in proc. of 15th International Symposium on Quality Electronic Design (ISQED), Mar. 2014, pp. 263 - 269.

[25] M.S.K Lau, K.V. Ling, and Y.C. Chu, ”Energy-aware probabilistic multiplier: design and analysis,” in proc. of international conference on Compilers, architecture, and synthesis for embedded systems, Oct. 2009, pp. 281- 290.