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HIGH PERFORMANCE VOLTAGE LEVEL SHIFTER USING DOUBLE CURRENT LIMITTER

Mr .K. MAHESH BABU[1], GUDUR SRI CHARAN[2], GURRAPPAGARI ASHA[3], KANDURI YASASWITHA[4], KATTUPUDI JAYA SUBRAMANYA BALAJI[5], GUNDULLURU GEETHIKA[6]

[1]Assistant Professor, Dept. of ECE, S V College of Engineering, Tirupati, A.P, India.

[23456]B.Tech Students,Dept. of ECE, S V College of Engineering, Tirupati, A.P, India.

ABSTRACT

Modern VLSI designs and IOT applications uses multi supply voltage design techniques for the purpose of trade off energy and speed. Level Shifters(LSs) are interfacing circuits that allow different voltage domains to be interfaced. In this project we propose a 0.125V – 0.325V input to 1.3V output-voltage Level Shifter that satisfies the requirement of Power, Delay and voltage level shifting requirements of Current IOT applications.

The design was achieved using strong current limiters and potency pull down network. The proposed LS was implemented using 130nm technology and incurs static power of 6.6nW propagation delay of 10ns at level shifting from 0.2V to 1.25V which is appropriate for IOT applications.

Keywords: IOT applications, Level Shifters, current limiters**.**

1. INTRODUCTION

Digital systems also have a variety of cases where two or more parts of the network work from separate voltages of the power supply. As signals cross the boundary between different power supply regions, a circuit block must be inserted which shifts the logic levels from, for example, the level supplied by one domain with a+5 Volt power supply to a sec. Level Shifter cell is used to transfer a set of signal voltages through one voltage domain to another. This is necessary when multiple voltage domains are operating on the chip. A signal that have a voltage spectrum in one voltage domain which is different from the signal in another voltage domain. This variation in the voltage range will cause the destination domain to work unreliably.

Low to High LSs can be realizable using buffers. Generally the gate voltage of MOS devices can be driven to the level of breakdown voltage. The breakdown voltage typically much greaterthan the power supply

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voltage, the input of the MOS device can be driven at higher voltage than supply voltage.

2. LITERATURE RIVEW OF LEVEL SHIFTER

The LS "An Ultra-Low Voltage-Level Shifter Using Revised Wilson Current Mirror for Fast and Energy-Efficient Wide-Range Voltage Conversion from Sub-Threshold to I/O Voltage" is a Wilson current mirror model. Wilson current mirror involves an input controlled diode and feedback control makes LS accomplishes small propagation delay and less power dissipation for wide voltage conversion from below threshold to I/O range.

It additionally utilizes "Mixed-device and Inverses narrow width device" sizing to improve the overall delay and power [3],[14].The LS [4] entitled "Low-Power Level Shifter for Multi Supply Voltage Designs is a modified DCVSL architecture" is the DCVSL model. In this paper novel, low-power LS for vigorous voltage shifting from the near or sub-threshold to the above threshold voltage is proposed. The design exploits design strategies to limit energy and static power. Because of these highlights, the proposed LS exhibits lower static power and energy.

The LS [5] entitled "Fast and Wide Range Voltage Conversion in Multi-supply Voltage Designs" is a crosscoupled Multi-Vt LS is depicted in fig. 2.3. In this paper new LS appropriate robust level shifting from the near or subthreshold to above-threshold is presented, which poses crosscoupled connections for achieving good power optimization. This method uses multiple supplies voltages to perform voltage level shifting, the estimated aspect ratio of NMOS to PMOS is approximately around 2400 to perform full functional DCVS converts 0.2V to 1V.

The LS in the designs [6], [7], [8], [9], [10] uses two stages, the primary one is a DCVSL with ON diode NMOS transistor, where the second stage is conventional DCVSL for achieving full voltage swing. Being dual stages DCVSL, the contention may arise due to this design may lead to poor speed performance.

3. EXISTING METHOD

Digital systems also have a variety of cases where two or more parts of the network work from separate voltages of the power supply. Different power supply regions, a circuit block must be inserted which shifts the logic levels from, for example, the level supplied by one domain with a+5 Volt

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This variation in the voltage range will cause the destination domain to work unreliably. Low to High LSs can be realizable using buffers. Generally the gate voltage of MOS devices can be driven to the level of breakdown voltage. The breakdown voltage typically much greater than the power supply voltage, the input of the MOS device can be driven at higher voltage than supply voltage.

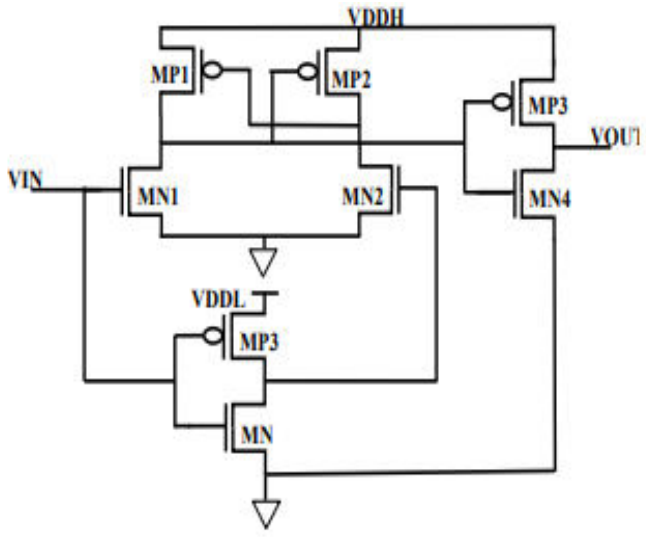

Fig. 1: DCVS Level Shifter

4. PROPOSED METHOD

The circuit current limiters MN1 and MN2 MOS transistors weaken the current contention of the pull-up network. When the voltage input VIN is at voltage low to voltage high transition, MOS transistor MN5 makes pull-down ON. This will invert the output by MN8-MP4 inverter with full swing output voltage VOUT. At VIN high to low voltage transition the possible short circuit current at the output inverter can increase. To avoid another pair of current limiters MN3-MN4 have introduced.

VIN is logic '1', i.e.as low as 0.15V, then MOS transistor MN5 turns ON and VDDL inverter MP3-MN7 produces a strong logic '0', will make MN6 OFF.

When MN6 is ON the driving inverter MP4-MN8 produces the strong logic '1', i.e. 1.25V through the pull-up MP4 ON. When the voltage swing is low in the main conversion stage and the current is limited through the current limiters MN1- MN2 and MN3-MN4 the better power consumption and delay could be able to achieve.

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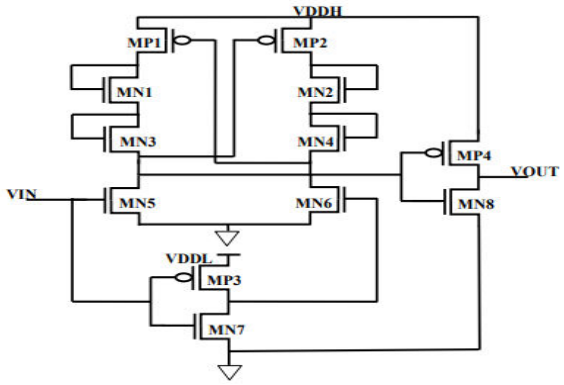

Fig. 3: The proposed Level shifter

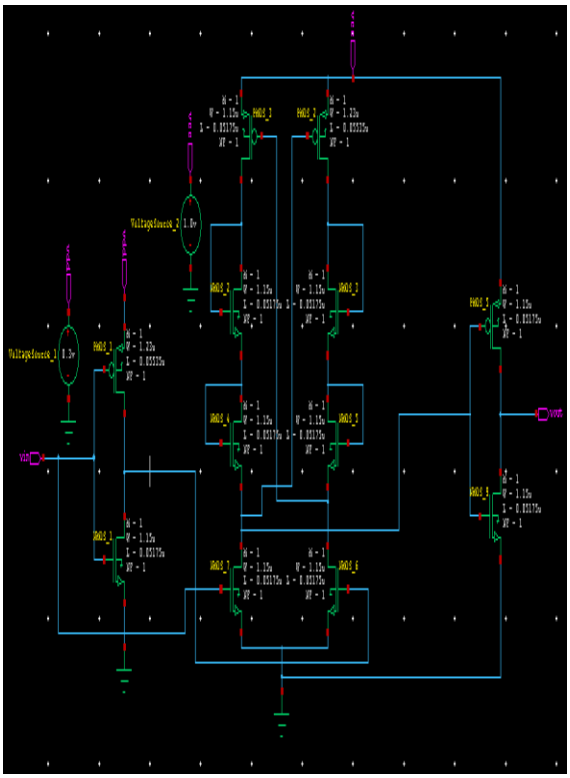

Fig. 4: The proposed Level shifter in Schematic Editor

5. METHODS OR TECHNIQUES USED IN OUR PROJECT

Tanner EDA :

Tanner EDA provides a complete line of software solutions for the design, layout and verification of analog and mixed-signal integrated circuits.

Tanner's solution consist of tools for schematic entry, circuit simulation, waveform probing, full-custom layout editing, placement and routing, netlist extraction, LVS and DRC verification.

6. RESULTS

Simulated results are performed in Tanner EDA tool using 45nm technology with 0.3V as the input voltage. The proposed Level Shifter circuit is evaluated and compared to the DCVS level shifter circuit. The power and delay obtained of the designs are summarized in the Table 1. The voltage input and output for proposed level shifter is shown in Fig 5.

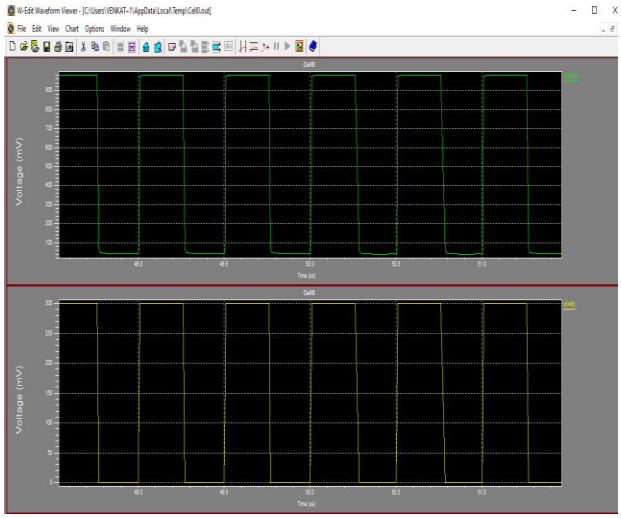

Fig. 5: Simulated output of the proposed Level Shifter

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Table. 1:Comparision between existing and proposed Level Shifter

Parameter	Existing level shifter	Proposed Level shifter
Power	4.41303mw	4.14276mw
Delay	13.425ns	2.9526ns

7. ADVANTAGES

1. High efficiency.
2. Power consumption is reduced.
3. High speed.

8. APPLICATIONS

1. Widely used in consumer electronics sector.
2. Enabled in the integration of various devices in a System on Chip.
3. IOT applications.

9. CONCLUSION

The proposed Current limiter circuit was designed using 45nm CMOS technology to perform the voltage level shifting from 0.3V to 1.0V. The results prove that the proposed circuit comfortably shifts at low power consumption.

The proposed design can be as robust because of the wide conversion range as well as meeting all the requirements of IoT requirements and its power consumption is of the best benchmark designs.

10. FUTURE SCOPE

A level shifter is also called voltage level translator is a circuit that translates signals from one logic level to another facilitating compatibility between ICs (Integrated circuits) with different voltage requirements such as Transistor-Transistor Logic (TTL) and Complementary Metal Oxide Semiconductor (CMOS). This technique is deployed to ensure that two connected devices with different operational voltages are compatible thereby being used to bridge domains between processors, logic, sensors and other circuitsnot leading to downtime. 1.8V, 3.3V, 5V are the most common voltage levels in TTL devices. Level shifters are an important part of electrical and digital devices.

Level shifter is widely used in consumer electronics sector as it enables the integration of various devices in System On Chip (SOC) ensuring fewer points of failure, proper drive strength and accurate timing during signal transition from one voltage level to another.

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