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Design of Different Multiplier Architectures for high-speed VLSI Circuits

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Abstract:
The paper focuses on improving the efficiency and performance of multipliers, which are vital components in microprocessors, DSPs (Digital Signal Processors), and quantum computers. The speed of a multiplier is crucial for determining the overall processor speed, and adders play a significant role in the performance of multipliers. The traditional Full Adder circuit, which typically consists of two EX-OR gates and two AND gates, is replaced with a multiplexer- based circuit in the proposed design. This modified Full Adder architecture is then used to implement different multiplier architectures, such as Array Multiplier, Wallace Tree Multiplier, Carry Save Multiplier, and Dadda Multiplier, using Verilog HDL (Hardware Description Language) for 4-bit and 8- bit input sizes. The designed multipliers are compared with existing multiplier architectures in terms of power consumptionand speed to assess their performance. The NEXYS 4 DDR FPGA Board is suggested as a potential platform for prototyping the designed multipliers. The designs are simulatedand synthesized using the VIVADO environment, and parameters such as delay and power obtained from the synthesis report are compared with other existing multipliers to evaluate their efficiency and performance.

Keywords—FPGA, Adders, Multipliers- Array, Carry Save,Dadda, Wallace Tree

I. INTRODUCTION

The invention of the transistor in 1947 by William B. Shockley and his colleagues at Bell Laboratories revolutionized the field of electronics, leading to the emergence of microelectronics as a new industry. Integrated circuits (ICs) were developed in the 1960s, which enabled multiple components to be integrated onto a single chip, making electronic devices smaller, more reliable, and more affordable. With advancements in technology, the number of devices per IC has increased rapidly, leading to the development of Very Large-Scale Integration (VLSI) technology. VLSI ICs, which contain over 105 transistors, have found widespread applications as general-purpose ICs such as microprocessors, memories, and DSPs, as well as application-specific ICs (ASICs). VLSI technology has revolutionized various industries and continues to drive innovation in areas such as AI, IoT, and wearables, shaping the future of electronics with increased functionality, performance, and power efficiency.

II. FULL ADDER

A. Traditional Full Adder

Full Adder is the adder that adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN. The output carry is designated as C-OUT and the normal output is designated as S which is SUM. A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to another. we use a full adder because when a carry-in bit is available, another 1-bit adder must be used since a 1-bit half-adder does not take a carry-in bit. A 1-bit full adder adds three operands and generates 2-bit results.

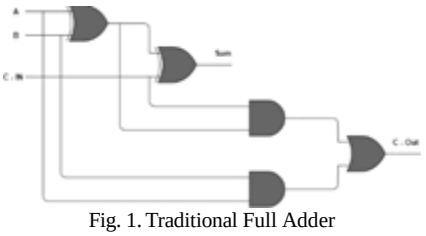

Fig. 1. Traditional Full Adder

B. Multiplexer based Full Adder

Multiplexer and Full adder are two different Digital Logic circuits. The Multiplexer is a digital switch. It allows digital information from several sources to be routed onto a single output line. On the other hand, the Full adder circuit performs the addition of three bits

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and produces the Sum and Carry as an output. Our aim is to build the Full Adder circuit using Multiplexers rather than the usual basic logic gates.

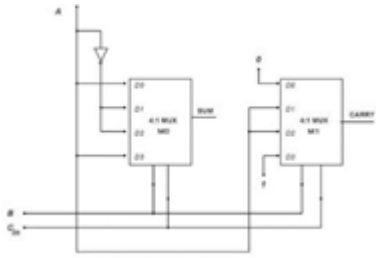

Fig. 2. MUX based Full Adder

III. MULTIPLIERS

To increase the speed multiplexer based full adder is used in the circuit Depending upon the type of application, the parallel or the serial multiplier can be used. Some of the known parallel multipliers are

1. Array multiplier
2. Carry Save Multiplier
3. Dadda Multiplier
4. Wallace Tree Multiplier

A. Array Multiplier

Array multiplier is an efficient layout of a combinational multiplier. Multiplication of two binary number can be obtained with one micro-operation by using a combinational circuit that forms the product bit all at once thus making it a fast way of multiplying two numbers since only delay is the time for the signals to propagate through the gates that forms the multiplication array.

Fig. 3. 4 X 4 Array Multiplier

B. Carry Save Multiplier

In a carry-save multiplier, carry-bits are not immediately added, but are rather “saved” for the next adder stage. In the final stage, carries and sums are merged in a fast carry- propagate adder stage (vector-merging adder). The carry-save multiplier structure is shown in the figure below.

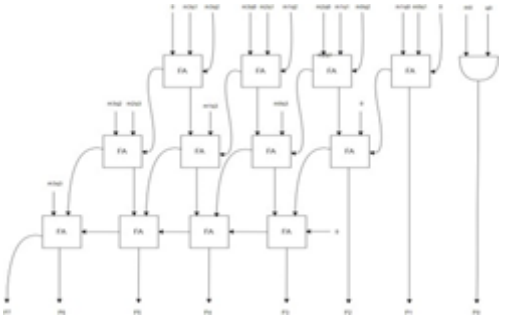

Fig. 4. 4 X 4 Carry Save Multiplier

C. Dadda Multiplier

The Dadda multiplier is a hardware binary multiplier design invented by computer scientist Luigi Dadda in 1965.It uses a selection of full and half adders to sum the partial products in stages (the Dadda tree or Dadda reduction) until two numbers are left. The design is similar to the Wallace multiplier, but the different reduction tree reduces the required number of gates (for all but the smallest operand sizes) and makes it slightly faster (for all operand sizes).

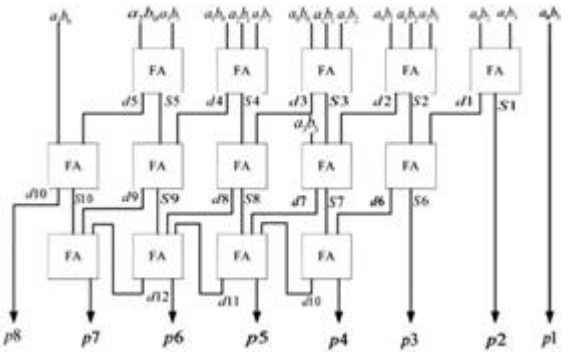

Fig. 5. 4 X 4 Dadda Multiplier

D. Wallace Tree Multiplier

A fast process for multiplication of two numbers was developed by Wallace. Using this method, a three-step process is used to multiply two numbers; the bit products are formed, the bit product matrix is reduced to a two-row matrix where sum of the row equals the sum of bit products, and the two resulting rows are summed with a fast adder to produce a final product.

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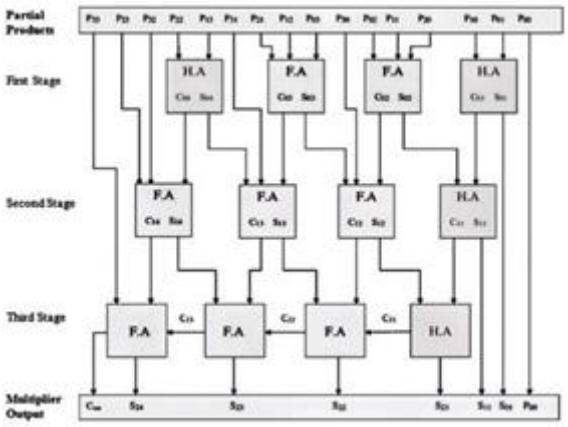

Fig. 6. 4 X 4 Wallace Tree Multiplier

IV. LITERATURE REVIEW

Many different adder architectures have been proposed for speeding up multipliers and making them high-speed VLSI circuits over the literature survey. Different adders are studied in which multiplexer based full adders are faster and effective.

A Competent Design of 2:1 Multiplexer and Its Application in 1-Bit Full Adder Cell [1], for low-leakage and high-speed circuit concern should be on both the factor speed and power this paper concluded with the efficient approach of multiplexer at 180nm technology. Modified differential cascade voltage switch logic (MDCVSL) shows least power consumption over a range of power supply voltage, power- delay product, operating frequency, output load capacitance and operating temperature over other circuit design of 2:1 multiplexer. The MDCVSL Based 1-bit full adder is found to give better performance than the NMOS based full adder. It shows remarkable improvement in power delay product and has better temperature sustainability. Hence MDCVSL multiplexer-based adder is suitable for lower power high- speed application. It has a marginal increase in area compared to the NMOS multiplexer-based adder; overall, we achieved the lowest power consumption and power delay product.

MUX based 1 Bit Full Adder Design [2], In this paper, the full adder designed using this 2T multiplexer based 1 Bit Full Adder is designed that found to be efficient from both speed and power perspective. Reduced number of transistors also helped in reducing the power dissipation and increasing the speed of the design.

Delay-Power Performance Comparison of Multipliers in VLSI Circuit Design [3], A typical processor central processing unit devotes a considerable amount of processing time in performing arithmetic operations, particularly multiplication operations. Multiplication is one of the basic arithmetic operations and it requires substantially more hardware resources and processing time than addition and subtraction. In fact, 8.72% of all the instruction in typical processing units is multiplication. In this paper, comparative study of different multipliers is done for low power requirement and high speed. The paper gives information of “Urdhva Tiryakbhyam” algorithm of Ancient Indian Vedic Mathematics which is utilized for multiplication to improve the speed, area parameters of multipliers. Vedic Mathematics suggests one more formula for multiplication of large number i.e., “Nikhilam Sutra” which can increase the speed of multiplier by reducing the number of iterations. High-Speed Area-Efficient VLSI Architecture of Three-Operand Binary Adder.

V. METHODOLOGY

The main objective of the paper is to identify the problem where the delay occurs and what effects the speed of the circuit and how the speed can be enhanced the speed of the multiplier defines the speed of the processor and it is not an easy task to enhance the speed. For that, a new modified version of Adder is proposed.

The conventional full adder in multipliers can be replaced with Multiplexer based full adder. In Multiplexer based full adder the full adder is implemented using 4:1 multiplexer. This implementation uses a two 4:1 MUX and one NOT gate. A transistor level implementation uses a total of 20 transistors which reduces area compared to conventional approach.

The modified version of full adder i.e., MUX based Full adder is implemented in different multiplier architectures like Array Multiplier, Carry Save Multiplier, Dadda Multiplier, Wallace Tree Multiplier for enhanced speed. The conventional Full Adder is replaced with modified full adder in all the mentioned multiplier architecture for increased speed. There is a more decreased delay when implemented this mux based full adder in 8-bit rather than 4-bit.

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VI. RESUTS

The designed multipliers i.e., conventional Array, Carry Save, Dadda, Wallace Tree Multipliers and Array, Carry Save, Dadda, Wallace Tree Multipliers using MUX based Full Adder (4-bit, 8-bit) are synthesized and also implemented using Xilinx VIVADO 2016.4. After synthesis and implementation process, the designer can view the RTL schematic, routed design on FPGA schematic and technology schematic, obtain the synthesis report which give information on area utilization of the design on the selected FPGA type, delay report, various timing reports and many more reports. Table 7.1 illustrates the comparison of the designed 4 multipliers in terms of delay (ns) and power(w).

TABLE I. COMPARISON OF 4-BIT MULTIPLIERS IN TERMS OF DELAY (NS) AND POWER(W)

4X4 Multipliers	**Parameters**			
	Delay (ns)		**Power (W)**	
	Normal	*Modified*	*Normal*	*Modified*
Array	10.292	10.070	3.985	3.192
Dadda	11.631	9.057	4.084	3.248
Carry Save	10.667	9.294	4.062	3.328
Wallace Tree	10.479	10.349	4.101	3.211

TABLE II. COMPARISON OF 8-BIT MULTIPLIERS IN TERMS OF DELAY (NS) AND POWER(W)

8X8 Multipliers	**Parameters**			
	Delay (ns)		**Power (W)**	
	Normal	*Modified*	*Normal*	*Modified*
Array	22.089	14.371	13.6	10.836
Dadda	16.216	11.662	13.187	10.635
Carry Save	16.994	12.938	13.599	10.925
Wallace Tree	19.389	17.428	13.337	10.704

VII. CONCLUSION

Numerous modified multipliers are found in literature. High speed VLSI has received too much consideration in the recent years. As a means of guaranteeing better performance, various multipliers are implemented with modified Full Adder. Adder implemented with MUX will usually be much faster than conventional adder and reduces the delay. This Adder is implemented in different multiplier architectures like Array Multiplier, Carry Save Multiplier, Dadda Multiplier and Wallace Tree Multiplier to improve efficiency. The performance of the different multiplier structures is evaluated by measuring the delay. Simulated and synthesized in VIVADO environment.

VIII. ACKNOWLEDGMENT

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