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DESIGN OF 8-BIT ALU DESIGN USING GDI TECHNIQUES WITH LESS POWER AND DELAY

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ABSTRACT—Arithmetic Logic Unit (ALU) is a substantial fragment of microchip. Cutting-edge computerized processors, legitimate and math activity accomplishes making use of ALU. This paper depicts an 8-Bit ALU operating with a lowest power 11-Transistor Full Adder (11-T FA) and Gate dispersion input (GDI) centered MUX. All structures were simulated using Tanner EDA software version-15 with 32 nanometer BSIM4 innovation. Execution examinations were furnished as for voltage, power, postponement and power delay item. In this paper 8-bit ALU operated in subthreshold region, selected 0.7 VDD for maintain the both power as well as delay. In 8-bit ALU of GDI proposed model, less than 82% power consumption reduced as compare with CMOS 8-Bit ALU due to voltage level improvement

INTRODUCTION The utilization of VLSI innovation has long-drawn-out to that level here a massive amount of transistors be able to be actualized in a solitary Bit. Complementary Metal Oxide Semiconductor (CMOS) remained the spine in blended sign as this one‟s diminishing force offers great blend segment for modest and computerized structure. The supports of intensity utilization in CMOS circuits are dynamic power (Pd), short out power (Psc) and static power (Ps). Along these lines, the complete power utilization (Pt) is Pt= Pd+ Psc + Ps (1) Pd expends because of capacitive burden in addition to clock recurrence. Psc is brought about by short out current. Ps is brought about by leakage current between the substrate and dispersion region. Expanding transistor quantityfor every chip territory plus scaling down advances have devoured additional power along these lines. The principle goal line is in the direction of decreasing the power utilization via employing unique approaches intended to improve the demonstration of Very Large Scale Integration circuits. Arithmetic Logic Unit is the segment of PC processor which accomplishes number-crunching as well as coherent activities [1]. ALU is a solely combinational rationale circuit whose yield deviates with altering information reaction.

PREVIOUS WORK Power diminishing could be achieved at Module Level or at circuit level or at architecture level [2]. In simple switch procedure select info rationale as control rationale and permits additional info signal from gate terminal [3]. Full Adder is a fundamental structure in place of planning an ALU. Various sorts of FA

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planning in place of limiting force are, for example, Hybrid Full Adder (H-FA) and 10 Transistor reduced power Full Adder (10T-FA) and 11 transistor FA (11T-FA) etc. FA works in mode of ultra-low through utilization of subthreshold current then expends low power [2], [3]. Full Adder is manufactured utilizing near to the ground power XOR gate and 2:1 multiplexer. ALU configuration employing FinFET innovation has dual gates that are electrically free. This limits the intricacy of the circuit and furthermore lessens the power utilization because of diminishing the leakage current. In Fin Field Effect Transistor (FinFET) innovation "Fin" is dainty silicon that shapes the frame of the gadget [4]. Arithmetic Logic Unit plan utilizing the re-configurable rationale of Multiple Input Floating Gate - Metal Oxide Semiconductor (MIFG-MOS) transistor has numerous information that expands the effectiveness of the circuit. MIFG-MOS transistor offers low and high conditions by watching theweighted aggregate of altogether things considered. MIFG-MOS transistor diminishes the quantity of transistors and the unpredictability with the circuit in addition to improving the exhibition of the circuit limit the postponement as well as diminishes the power dissemination [5]. AT the point where channel size is scaled discouraged for organizing the circuits, Gate of metal and higher value dielectric K are to be advertised

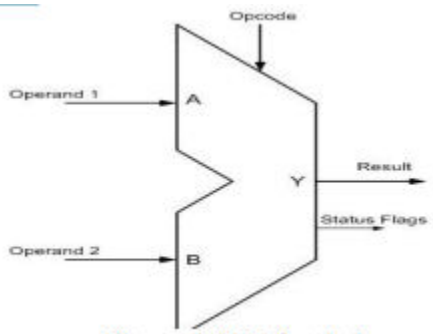

Figure 1. ALU Symbol

LITERATURE SURVEY

There are different types and designs of full adder which is discussed in various papers at state of the art level andprocess and circuit level. Twelve state of the art full adder cells are: conventional CMOS, CPL, TFA, TG CMOS,C2MOS, Hybrid, Bridge, FA24T, NCell, DPL and Mod2f. R. Shalem, E. John, and L.K. John, proposed a conventionalCMOS full adder consisting of 28 transistors [1]. Later, the number of transistor count is reduced to have less area andpower consumption. A. Sharma, R Singh and R. Mehra, Member, IEEE, have improved performance with Transmission Gate Full adder using CMOS nano technology where 24 transistors are used [2]. The Complementary Passtransistor Logic (CPL) full Adder contains the 18 transistors. The power consumption of this structure is 2.5µw [3].A Transmission Function Full Adder (TFA) based on the transmission function theory has 16 transistors. The powerconsumption of this structure is 12µw. NCELL contains the 14 transistors and utilizes the low power XOR/XNOR circuit. The power consumption of this structure is 1.62µw. Mod2f Full Adder contains the 14 transistors, generates full swing XOR and XNOR signals by utilizing a pass transistor

based DCVS circuit. The power consumption of this structure is 2.23μw [3]. Saradindu Panda, N. Mohan Kumar, C.K. Sarkar, optimized the full adder circuit to 18 Transistorusing Dual Threshold Node Design with Submicron Channel Length [4]. T. Vigneswaran, B. Mukundhan, and P.Subbarami Reddy, designed 14 transistor high speed CMOS full adder and significantly improved threshold problem to50% [5]. Gate Diffusion Input Technique is a new method of reducing power dissipation, propagation delay with less area.T. Esther Rani, M. Asha Rani, Dr.RameshwarRao, designed an area optimized low power arithmetic and logic unit inwhich Arithmetic Logic Unit is implemented using logic gates, pass transistor logic, as well as GDI technique [6].Manish Kumar, Md. Anwar Hussain, and L.L.K. Singh explained a Low Power High Speed ALU in 45nm UsingGDI Technique and Its Performance Comparison [7]. We have designed ALU in different way by using GDIcells to implement multiplexers and full adder circuit. The input and output sections consist of 4x1 and 2x1 multiplexersand ALU is implemented by using full adder.

R. Shalem, E. John, and L.K.John, "A novel low-power energy recovery full adder cell," in Proc. Great Lakes Symp.VLSI,Feb. 1999, pp.380–383.

Design of complex arithmetic logic circuits considering active power and delay is an important and challenging task in deep submicron circuits. Double gate transistor circuit consider as a promising candidate for low power application domain as well as used in Radio Frequency (RF) devices. In this paper we designed full adder with the help of double gate transistor, the used parameters value has been varied significantly thus improving the performance of full adder. Power Gating is one of the most used circuit techniques to reduce the leakage current in idle circuit. In this paper different parameters are analysed on Power Gating Technique. In double gate MOSFET (DGMOSFET), Si channel is very small in width and can be controlled by applying gate control on both sides of channel. In double gate device both gate are coupled each other and this reduce the short channel effect and leakage. By using two gates circuit with double gate transistor can be operated as low input voltage as compared to the planer CMOS circuit and these means low power consumption. Gate leakage is also low in double gate device. It is occur due to gate tunnelling and overlap tunnelling current. Here short channel effect is controlled by two gates so there is no need to heavy doping. Since very light doped or undopped channel can be used in double gate transistors.

Design and Analysis of Low-Power 11-Transistor Full Adder

Full adders are exigent components in applications such as digital signal processors (DSP) architectures and microprocessors. In this paper, we propose a technique to build a new 11-transistor FA .We have done HSPICE simulation runs the new design 11-T full adders .In CMOS integrated circuit design there is a tradeoff between static

power consumption and technology scaling. Static power dissipation is a challenge for the circuit designer. So we reduce the static power dissipation. In order to achieve lower static power consumption, one has to scarifies design area and circuit performance. In this paper we propose a new circuit of 11-Transistor full adder in CMOS VLSI circuit.

L.Bisdounis, D.Gouvetas and O.Koufopavlou, "A comparative study of CMOS circuit design styles for low power high-speed VLSI circuits" Int. J. of Electronics, Vol.84, No.6, pp 599-613,1998. Anu Gupta, Design Explorations of VLSI Arithmetic Circuits, Ph.D. Thesis, BITS, Pilani, India, 2003. In this paper we presents a implementation of area and power efficient 4 bit Arithmetic And Logic unit (ALU) through concept of gate diffusion input (GDI) technique. ALU is most important and core component of CPU.ALU is also used as core component of number of embedded and microprocessor systems. ALU consists of 4x1 multiplexer, 2x1 multiplexer, full adder .These are designed to implement different logical and arithmetic operations such as AND, OR, ADD, SUBTRACT etc. The 4x1 multiplexer, 2x1 multiplexer, full adder are implemented through GDI cells. These are associated to realize 4 bit ALU. The simulation is carried out based on MENTOR GRAPHICS 130nm technologies and compared with pass transistor and CMOS logic realization. The simulation gives that design of ALU through GDI is more efficient with low power consumption, occupies less surface area and faster compared with pass transistor and CMOS logic.

PROPOSED SYSTEM

An arithmetic logic unit (ALU) is a fundamental building block of the Central Processing Unit (CPU) of a computer, and even the simplest microprocessors contain one. It is responsible for performing arithmetic and logic operations such as addition, subtraction, increment, and decrement, logical AND, logical OR, logical XOR and logical XNOR. ALU consists of eight 4x1 multiplexers, four 2x1multiplexers and four full adders. The 4-bit ALU is designed in 250nm, n-well CMOS technology. When logic '1'and logic '0' are applied as an input INCREMENT and DECREMENT operations takes place respectively. An INCREMENT operation is analyzed as adding '1' to the addend and DECREMENT is seen as a subtraction operation. Two's complement method is used for SUBTRACTION in which complement of B is used. The outputs obtained from the full adder are SUM, EXOR, EXNOR, AND & OR. Fig. 6 shows the block diagram of 4-bit ALU where first stage to fourth stage is cascaded with the CARRY bit. Symbolic representation of 4-bit ALU has been visualized in fig. 7. The multiplexer stage selects the appropriate inputs based on the condition of the select signals, and gives it to the full adder which then computes the results.

The multiplexer at the output stage selects the appropriate output and route it to output port. Table II shows the truth table for the

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operations performed by the ALU based on the status of the select signal. The operation being performed and the inputs and outputs being selected are determined by set of three select signals incorporated in the design. Fig8 shows multiplex erlogic at input port and Fig 9. shows multiplexer logic at output port. The multiplexer stage selects the appropriate inputs based on the condition of the select signals, and gives it to the full adder which then computes the results. The multiplexer at the output stage selects the appropriate output and route it to output port. Table 2 shows the truth table for the operations performed by the ALU based on the status of the select signal

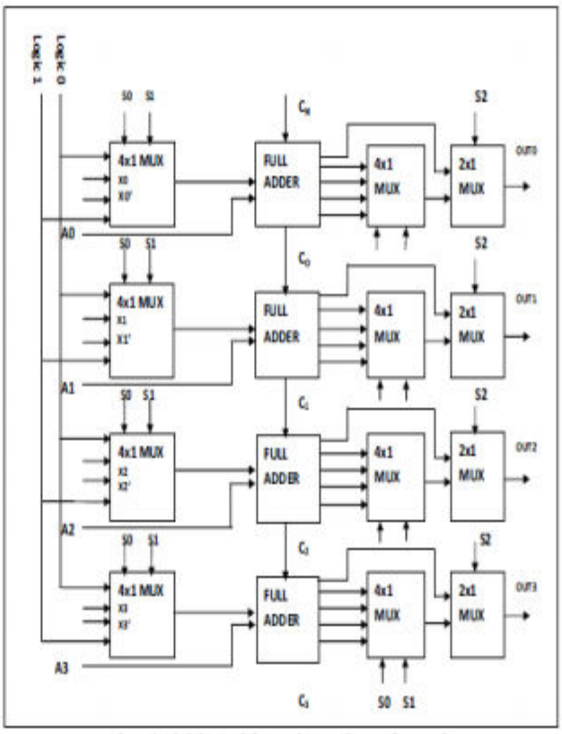

Fig.6. 4-bit Arithmetic and Logic Unit.

The schematic of ALU is designed using schematic editor of DSCH3.5 and Micro wind 3.5. It shows connectivity between the components and describes aspect ratios of the transistor that can be modified along with the design. Fig. 10 represents the complete schematic view of ALU. The 4-bit ALU consists of two 4-bit inputs, three selecting lines, and one carry input, one carry output and four output bits.

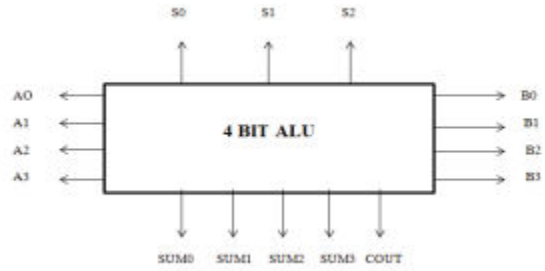

Fig.8.Symbol of 4-bit ALU.

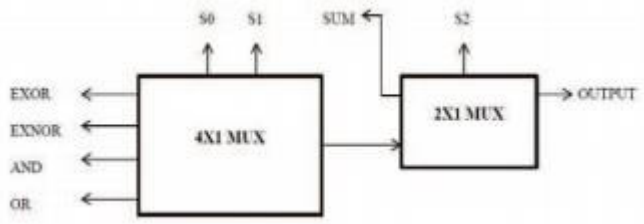

Fig.9. Block diagram of multiplexer logic at the output stage.

This paper presents a new approach using concept of Gate Diffusion Input Technique to design an arithmetic and logic unit. In an ALU, for appropriate selection of input to perform particular operation and for obtaining output accordingly multiplexer is the most applicable device. In earlier designs of ALU, the multiplexer unit is either implemented by conventional CMOS logic or by pass transistor logic which proven to have high power consumption. The approach gives better result than previous designs in terms of power

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consumption, propagation delay as well as area.

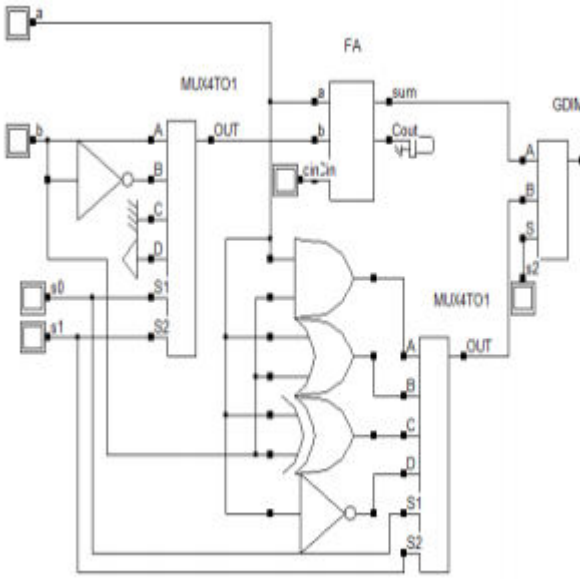
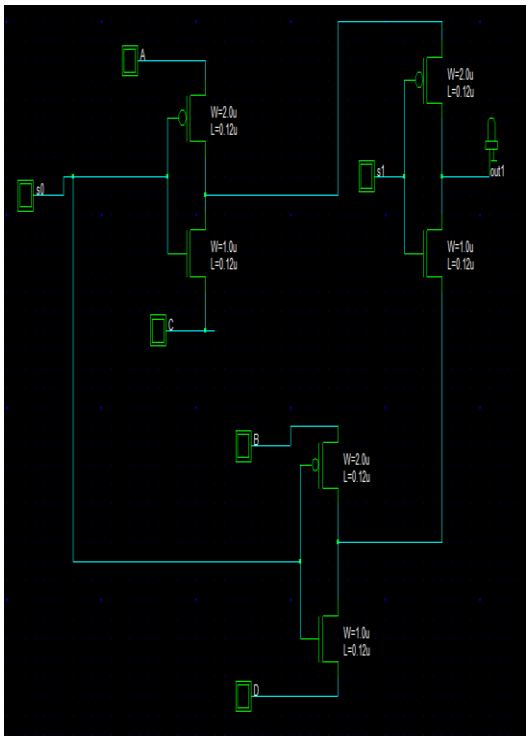
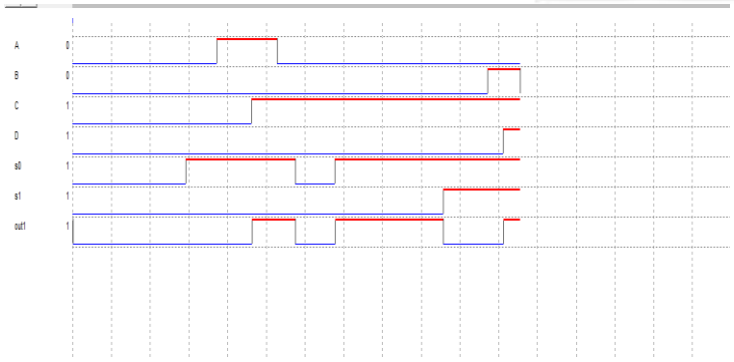


Fig.10. Schematic of 1-bit ALU.

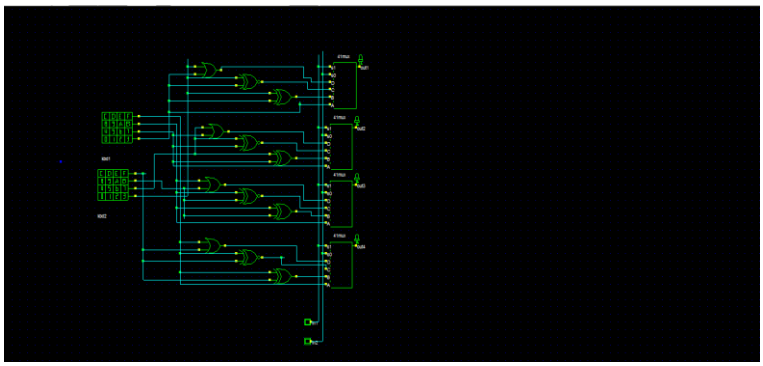
SIMULATION RESULTS

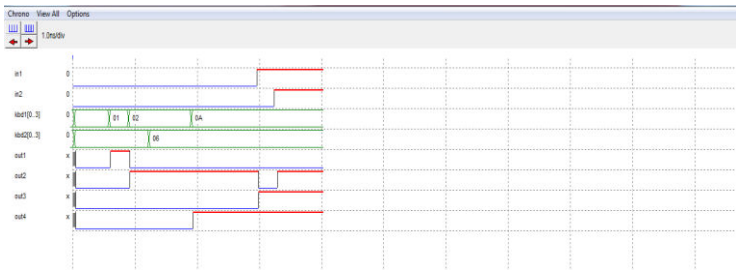
4*1mux:



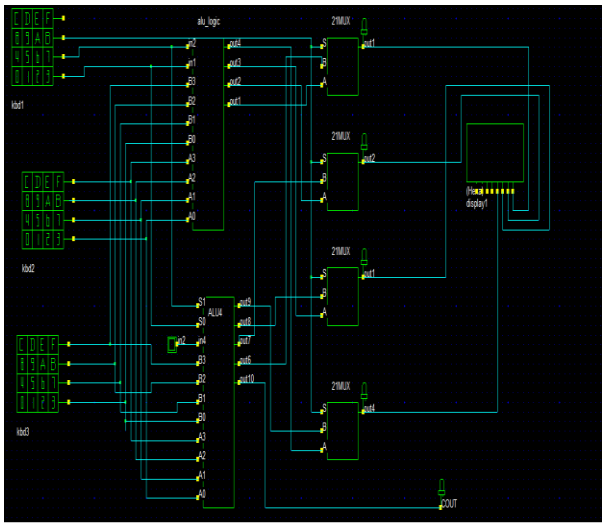


ALU





FINAL ALU



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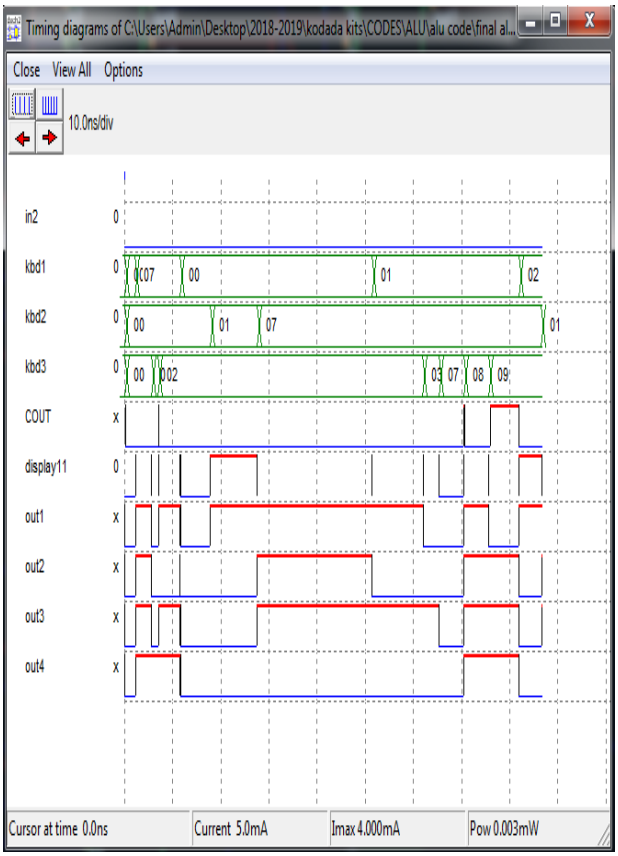

APPLICATIONS & ADVANTAGES

APPLICTIONS

- Processor applications
- Communicating applications
- Addition applications

ADVANTAGES

- low power
- less area based on less number of transisters
- less delay

CONCLUSION

Power consumption in CMOS circuit is classified in two categorize: static power dissipation and dynamic power dissipation. In today's CMOS circuit's static power dissipation is negligible thus not considered as compared to dynamic power dissipation. Dynamic Power dissipation in a CMOS circuit is given by P = CLf VDD2. The power supply is directly related to dynamic power. The numbers of power supply to ground connections are reduced in GDI implementation which reduces the dynamic power consumption. This work presents a 4-bit ALU designed in250nm technology for low power and minimum area with GDI technique. Various topologies of multiplexer and full adder implementation is studied and compared. The 2x1multiplexer, 4x1 multiplexer, 1-bit full adder with 10-transistors designed using GDI technique is chosen for lowering power consumption and minimum possible area. Power dissipation, propagation delay and the number of transistors of ALU were compared using CMOS, n MOSPTL and GDI techniques. GDI technique proved to have best result in terms of performance characteristics among all the design techniques.

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