International Journal For Recent Developments in Science & Technology
Crossref
A Peer Reviewed Research Journal

AHL & NBTI Calculation using reliable multiplier

Dr.M.Surendra Kumar,

Professor, Department of ECE,

KLR college of Engineering and technology-paloncha.

Abstract: - *Digital multipliers are among the most critical arithmetic functional units. The overall performance of the Digital multiplier systems depends on throughput of the multiplier. The negative partialness temperature instability effect occurs when a pMOS transistor is under negative inequitableness (Vgs = −Vdd), incrementing the threshold voltage of a pMOS transistor and reducing the multiplier celerity. Similarly, positive inequitableness temperature instability occurs when an nMOS transistor is under positive partialness. Both effects degrade the celerity of the transistor and in the long term, the system may be fail due to timing contravention. Ergo, it is required to design reliable high-performance multipliers. In this paper, we implement an agingaware multiplier design with a novel adaptive hold logic (AHL) circuit. The multiplier is able to provide the higher throughput through the variable latency and can adjust the adaptive hold logic (AHL) circuit to abate performance degradation that is due to the aging effect. The proposed design can be applied to the column bypass multiplier.*

Keywords*: - Adaptive hold logic (AHL), negative bias temperature instability (NBTI), positive bias temperature instability (PBTI), reliable multiplier, variable latency.*

1. INTRODUCTION

Digital multipliers are among the most critical arithmetic functional units in many applications, such as the Fourier transform, discrete cosine transforms, and digital filtering. The throughput of these applications depends on multipliers, and if the multipliers are too slow, the performance of entire circuits will be reduced. Furthermore, negative inequitableness temperature instability (NBTI) occurs when a pMOS transistor is under negative inequitableness (Vgs = −Vdd). In this situation, the interaction between inversion layer apertures and hydrogen-passivated Si atoms breaks the Si–H bond engendered during the oxidation process, engendering H or H2 molecules. When these molecules diffuse away, interface traps are left. The accumulated interface traps between silicon and the gate oxide interface result in incremented threshold voltage (Vth), reducing the circuit switching haste. When the partial voltage is abstracted, the inversion reaction occurs, reducing the NBTI effect. However, the inversion reaction does not eliminate all the interface traps engendered during the stress phase, and Vth is incremented in the long term. Hence, it is consequential to design a reliable high-performance multiplier. The corresponding effect

International Journal For Recent Developments in Science & Technology
2581-4575
Crossref
A Peer Reviewed Research Journal

on an nMOS transistor is positive partialness temperature instability (PBTI), which occurs when an nMOS transistor is under positive inequitableness. Compared with the NBTI effect, the PBTI effect is much more diminutive on oxide/polygate transistors, and ergo is customarily ignored. However, for high-k/metal-gate nMOS transistors with paramount charge trapping, the PBTI effect can no longer be ignored. In fact, it has been shown that the PBTI effect is more paramount than the NBTI effect on 32-nm high-k/metal-gate processes A traditional method to mitigate the aging effect is overdesign including such things as sentinel-banding and gate oversizing; however, this approach can be very pessimistic and area and power inefficient. To evade this quandary, many NBTI-vigilant methodologies have been proposed. An NBTI-cognizant technology mapping technique was proposed in to assure the performance of the circuit during its lifetime. In an NBTI-cognizant slumber transistor was designed to reduce the aging effects on pMOS slumber-transistors, and the lifetime stability of the potency-gated circuits under consideration was amended. Wu and Marculescu proposed a joint logic restructuring and pin reordering method, which is predicated on detecting functional symmetries and transistor stacking effects. They withal proposed an NBTI optimization method that considered path sensitization . In dynamic voltage scaling and body-predicating techniques were proposed to reduce power or elongate circuit life. These techniques, however, require circuit modification or do not provide optimization of categorical circuits. Traditional circuits use critical path delay as the overall circuit clock cycle in order to perform correctly. However, the probability that the critical paths are activated is low. In most cases, the path delay is shorter than the critical path. For these noncritical paths, utilizing the critical path delay as the overall cycle period will result in consequential timing waste. Hence, the variable-latency design was proposed to reduce the timing waste of traditional circuits. The variable-latency design divides the circuit into two components: 1) shorter paths and 2) longer paths. Shorter paths can execute correctly in one cycle, whereas longer paths need two cycles to execute. When shorter paths are activated

2. RELATED WORK

Subsisting system

A 4BIT ARRAY MULTIPLIER.

The composition of an array multiplier is shown in the figure BELOW..There is a one to one topological correspondence between this hardware structure and the manual multiplication shown in figure multiplication method.. The generation of n

2581-4575
International Journal For Recent Developments in Science & Technology
Crossref
A Peer Reviewed Research Journal

partial products requires N*M two bit AND gates. Most of the area of the multiplier is allegiant to the integrating of n partial products, which requires N-1, M-bit adders. The shifting of the partial products for their felicitous alignment's performed by simple routing and does not require any logic. The over all structure can be facilely be compacted into rectangle, resulting in very efficient layout.

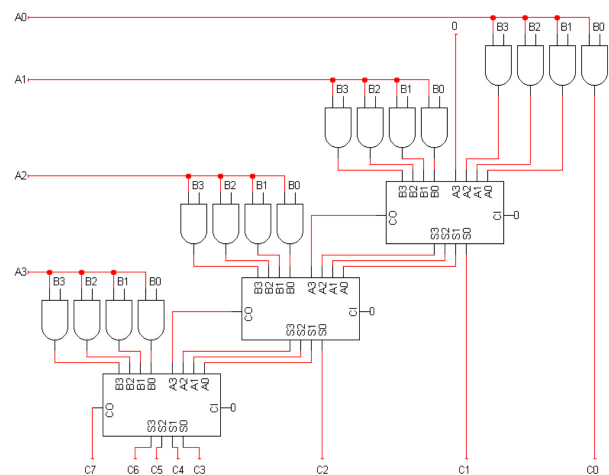

Fig:-1 Circuit

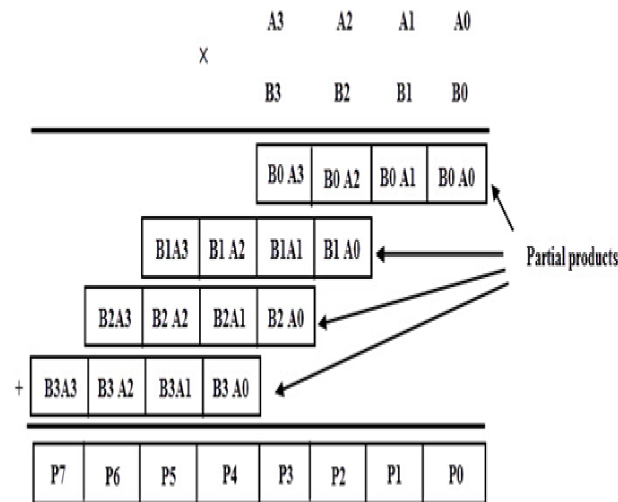

Fig:-2 Multiplication process

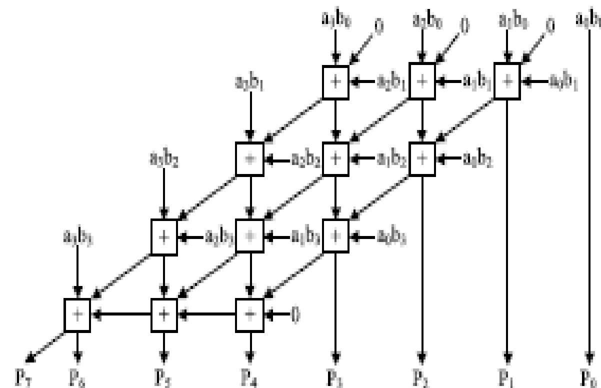

Fig:-3 circuit diagram

Mundane array multiplier.

A binary multiplier is an electronic circuit used I n digital electronics, such as a computer, to multiply two binary numbers. A variety of computer arithmetic techniques can be used to implement a digital multiplier. Most techniques involve computing a set of partial products, and then summing the partial products together. This process is kindred to the method edified to primary school children for conducting long multiplication on base-10 integers, but has been modified here for application to a base-2 (binary) numeral system. The first stage of most multipliers involves engendering the partial products which is nothing but an array of AND gates. An n-bit by n-nit multiplier requires n2AND gates for partial product generation. The partial products are then integrated to give the final results. A 4x4 array multiplier has been shown in figure:

Traditional circuits use critical path delay as the overall circuit clock cycle in order to perfor correctly. However, the probability that the critical paths are activated is low. In most cases, the path delay is shorter than the critical path. For these noncritical paths, utilizing the critical path delay as the overall cycle period will result in consequential timing waste. Hence, the variable-latency design was proposed to reduce the timing waste of traditional circuits.

Disadvantages

- Circuit arrangement is involute for more number of bit multiplier.
- Delay will be sizably voluminous due to ripple carry propagation.
- Cost of designed circuit is high.
- Speed performance of this system is low.

Proposed method

Reliable Multiplier Design with Adaptive Hold Logic

Proposed Architecture

This section details the proposed aging-cognizant reliable multiplier design. It introduces the overall architecture and the functions of each component and additionally describes how to design AHL that adjusts the circuit when consequential aging occurs. Fig. shows our proposed aging-vigilant multiplier architecture, which includes two m-bit inputs (m is a positive number), one 2m-bit output, one column- or row-bypassing multiplier, 2m 1-bit Razor flip-flops and an AHL circuit.

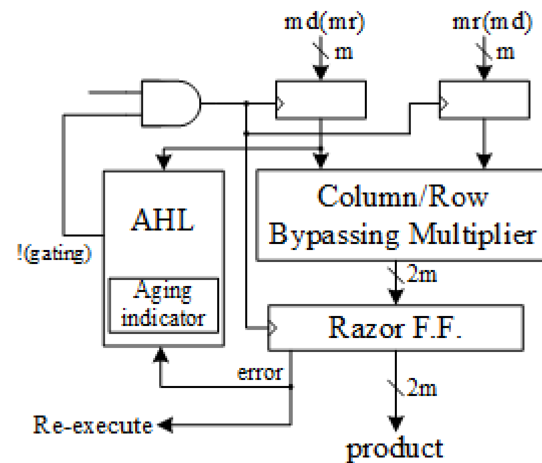

Fig:-4 Proposed architecture (md means multiplicand; mr means multiplicator) circuit

The details of Razor flip-flops. A 1-bit Razor flip-flop contains a main flip-flop, shadow latch, XOR gate, and mux. The main flip-flop catches the execution result for the combination circuit using a normal clock signal, and the shadow latch catches the execution result using a delayed clock signal, which is slower than the normal clock signal. If the latched bit of the shadow latch is different from that of the main flip-flop, this means the path delay of the current operation exceeds the cycle period, and the main flip-flop catches an incorrect result. If errors occur, the Razor flip-flop will set the error signal to 1 to notify the system to reexecute the operation and notify the AHL circuit that an error

2581-4575

International Journal For Recent Developments in Science & Technology

Crossref

A Peer Reviewed Research Journal

has occurred. We use Razor flip-flops to detect whether an operation that is considered to be a one-cycle pattern can really finish in a cycle. If not, the operation is reexecuted with two cycles. Although the reexecution may seem costly, the overall cost is low because the reexecution frequency is low. More details for the Razor flip-flop can be found in. The AHL circuit is the key component in the aging-ware

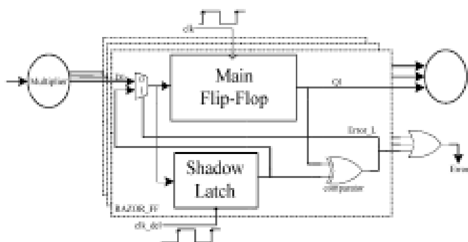

Fig:-5 Razor flips flops

Variable-latency multiplier. of the AHL circuit. The AHL circuit contains an aging indicator, two judging blocks, one mux, and one D flip-flop. The aging indicator indicates whether the circuit has suffered significant performance degradation due to the aging effect. The aging indicator is implemented in a simple counter that counts the number of errors over a certain amount of operations and is reset to zero at the end of those operations.

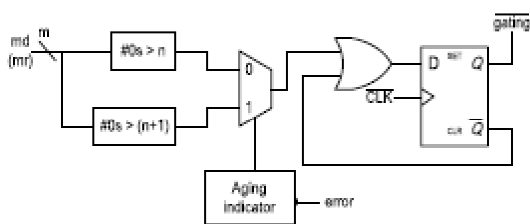

Fig:-6 Diagram of AHL (md means multiplicand; mr means multiplicator

If the cycleperiod is too short, the column- or row-bypassing multiplier is not able to consummate these operations prosperously, causing timing contravention. These timing contravention will be caught by the Razor flip-flops, which engender error signals. If errors transpire frequently and exceed a predefined threshold, it signifies the circuit has suffered consequential timing degradation due to the aging effect, and the aging designator will output signal 1; otherwise, it will output 0 to betoken the aging effect is still not paramount, and no actions are needed. The first judging block in the AHL circuit will output 1 if the number of zeros in the multiplicand (multiplicator for the row-bypassing multiplier) is more sizably voluminous than n and the second judging block in the AHL circuit will output 1 if the number of zeros in the multiplicand (multiplicator) is more astronomically immense than n + 1. They are both employed to decide whether an input pattern requires one or two cycles, but only one of them will be culled at a time. In the commencement, the aging effect is not consequential, and the aging bespeaker engenders 0, so the first judging block is utilized. After a period of time when the aging effect becomes consequential, the second judging block is opted

for. Compared with the first judging block, the second judging block sanctions a more diminutive number of patterns to become one-cycle patterns because it requires more zeros in the multiplicand (multiplicator). The details of the operation of the AHL circuit are as follows: when an input pattern arrives, both judging blocks will decide whether the pattern requires one cycle or two cycles to consummate and pass both results to the multiplexer. The multiplexer culls one of either result predicated on the output of the aging bespeaker. Then an OR operation is performed between the result of the multiplexer, and the .Q signal is utilized to determine the input of the D flip-flop. When the pattern requires one cycle, the output of the multiplexer is 1. The !(gating) signal will become 1, and the input flip flops will latch incipient data in the next cycle. On the other hand, when the output of the multiplexer is 0, which designates the input pattern requires two cycles to consummate, the OR gate will output 0 to the D flip-flop. Consequently, the !(gating) signal will be 0 to incapacitate the clock signal of the input flip-flops in the next cycle. Note that only a cycle of the input flip-flop will be incapacitated because the D flip-flop will latch 1 in the next cycle. The overall flow of our proposed architecture is as follows: when input patterns arrive, the column- or row-bypassing multiplier, and the AHL circuit execute simultaneously. According to the number of zeros in the multiplicand (multiplicator), the AHL circuit decides if the input patterns require one or two cycles. If the input pattern requires two cycles to consummate, the AHL will output 0 to incapacitate the clock signal of the flip-flops. Otherwise, the AHL will output 1 for mundane operations. When the column- or row-bypassing multiplier culminates the operation, the result will be passed to the Razor flip-flops. The Razor flip-flops check whether there is the path delay timing contravention. If timing breaches occur, it signifies the cycle period is not long enough for the current operation to consummate and that the execution result of the multiplier is erroneous. Thus, the Razor flip-flops will output an error to apprise the system that the current operation needs to be reexecuted utilizing two cycles to ascertain the operation is veridical.In this situation, the extra reexecution cycles caused by timing infringement incurs a penalty to overall average latency. However, our proposed AHL circuit can accurately prognosticate whether the input patterns require one or two cycles in most cases. Only a few input patterns may cause a timing variation when the AHL circuit judges incorrectly. In this case, the extra reexecution cycles did not engender consequential timing degradation. In

2581-4575
International Journal For Recent Developments in Science & Technology
Crossref
A Peer Reviewed Research Journal

summary, our proposed multiplier design has three key features. First, it is a variable-latency design that minimizes the timing waste of the noncritical paths. Second, it can provide reliable operations even after the aging effect occurs. The Razor flip-flops detect the timing contravention and reexecute the operations utilizing two cycles. Determinately, our architecture can adjust the percentage of one-cycle patterns to minimize performance degradation due to the aging effect. When the circuit is aged, and many errors occur, the AHL circuit utilizes the second judging block to decide if an input is one cycle or two cycles.

3. EXPERIMENTAL RESULTS

Fig:-7 Processer

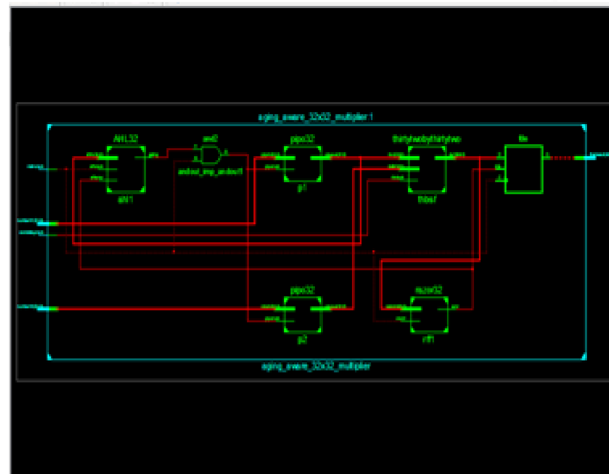

Fig:-8 Circuit

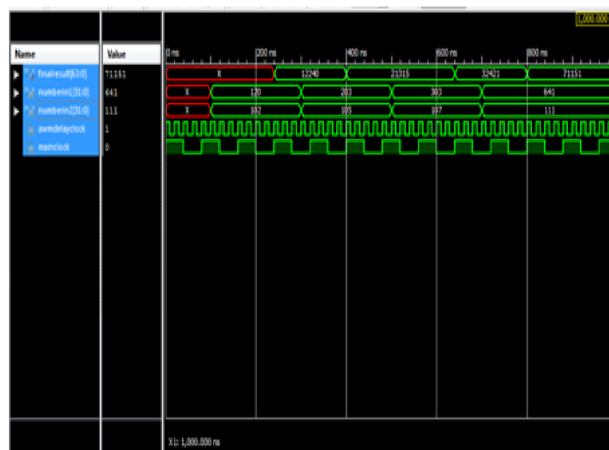

Fig:-9 Simulator Result

4. CONCLUSION

This paper proposed an aging-cognizant variable-latency multiplier design with the AHL. The multiplier is able to adjust the AHL to mitigate performance degradation due to incremented delay. The experimental results show that our proposed architecture with 16×16 and 32×32 columnbypassing multipliers can procure up to 62.88% and 76.28% performance amendment

compared with the 16 × 16 and 32 × 32 FLCB multipliers, respectively. Furthermore, our proposed architecture with the 16×16 and 32×32 rowbypassing multipliers can achieve up to 80.17% and 69.40% performance amendment compared with the 16 × 16 and 32 × 32 FLRB multipliers. In additament, the variable-latency bypassing multipliers exhibited the lowest average EDP and achieved up to 10.45% EDP reduction in 32 × 32 VLCB multipliers. Note that in additament to the BTI effect that increments transistor delay, interconnect additionally has its aging issue, which is called electromigration. Electromigration occurs when the current density is high enough to cause the drift of metal ions along the direction of electron flow. The metal atoms will be gradually displaced after a period of time, and the geometry of the wires will transmute. If a wire becomes narrower, the resistance and delay of the wire will be incremented, and in the terminus,electromigration may lead to open circuits. This issue is withal more solemn in advanced process technology because metal wires are narrower, and transmutes in the wire width will cause more immensely colossal resistance differences. If the aging effects caused by the BTI effect and electromigration are considered together, the delay and performance degradation will be more consequential. Auspiciously, our proposed variable latency multipliers can be used under the influence of both the BTI effect and electromigration. In integration, our proposed variable latency multipliers have less performance degradation because variable latency multipliers have less timing waste, but traditional multipliers need to consider the degradation caused by both the BTI effect and electromigration and utilize the worst case delay as the cycle period

5. REFERENCES

[1] Y. Cao. (2013). *Predictive Technology Model (PTM) and NBTI Model* [Online]. Available: http://www.eas.asu.edu/~ptm

[2] S. Zafar *et al.*, “A comparative study of NBTI and PBTI (charge trapping) in SiO2/HfO2 stacks with FUSI, TiN, Re gates,” in *Proc. IEEE Symp. VLSI Technol. Dig. Tech. Papers*, 2006, pp. 23–25.

[3] S. Zafar, A. Kumar, E. Gusev, and E. Cartier, “Threshold voltage instabilities in high-k gate dielectric stacks,” *IEEE Trans. Device Mater. Rel.*, vol. 5, no. 1, pp. 45–64, Mar. 2005.

[4] H.-I. Yang, S.-C. Yang, W. Hwang, and C.-T. Chuang, “Impacts of NBTI/PBTI on timing control circuits and degradation tolerant design in nanoscale CMOS SRAM,” *IEEE Trans. Circuit Syst.*, vol. 58, no. 6, pp. 1239–1251, Jun. 2011.

[5] R. Vattikonda, W. Wang, and Y. Cao, “Modeling and miimization of pMOS NBTI effect

for robust naometer design," in *Proc. ACM/IEEE DAC*, Jun. 2004, pp. 1047–1052.

[6] H. Abrishami, S. Hatami, B. Amelifard, and M. Pedram, "NBTI-aware flip-flop characterization and design," in *Proc. 44th ACM GLSVLSI*, 2008, pp. 29–34

[7] S. V. Kumar, C. H. Kim, and S. S. Sapatnekar, "NBTI-aware synthesis of digital circuits," in *Proc. ACM/IEEE DAC*, Jun. 2007, pp. 370–375.

[8] A. Calimera, E. Macii, and M. Poncino, "Design techniqures for NBTItolerant power-gating architecture," *IEEE Trans. Circuits Syst., Exp. Briefs*, vol. 59, no. 4, pp. 249–253, Apr. 2012.

[9] K.-C. Wu and D. Marculescu, "Joint logic restructuring and pin reordering against NBTI-induced performance degradation," in *Proc. DATE*, 2009, pp. 75–80.

[10] Y. Lee and T. Kim, "A fine-grained technique of NBTI-aware voltage scaling and body biasing for standard cell based designs," in *Proc. ASPDAC*, 2011, pp. 603–608.