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Power and Area Efficient 10T SRAM with improved Read Stability

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Abstract
In this paper, a 10T Static Random Access Memory bit cell is proposed to meet design specification for performance, stability, area and power consumption. In every state of SRAM cell designs low power and increased noise margin plays an important role. The conventional 6T SRAM cell is very much prone to noise during read operation. In order to overcome the Read SNM problem in the 6T SRAM cell designers have implemented many other SRAM configurations such as 8T, 9T, 10T. These SRAM cell configurations improve the read stability but increase the power consumption. We proposed a 10T SRAM cell which can solve all these problems by introducing the transmission gate and using stacking effect in the configuration. In this paper different SRAM cells analyzed on the basis of power and read stability and we proposed a 1-bit SRAM memory array using the proposed 10T SRAM bit cell that achieves cell stability, lower power consumption and lesser area. The proposed circuit was implemented in Mentor Graphics Design Architect, simulated using Mentor Graphics ELDO at supply voltage of 1.8V with the help of TSMC 180nm technology. Micro wind is used to draw layout of SRAM cells and peripherals.

Keywords:
Static Random Access Memory, Static Noise Margin, Read Static Noise Margin, Power Consumption, 10T SRAM

1. INTRODUCTION

Currently more than 50% of the area of System-on-Chip designs is occupied by embedded memory [1]. This is mainly due to the increased integration of functional blocks which require large memories for storage and data manipulation. There are many important aspects for SRAM cell designs: the cell area, cell stability and power consumption. The cell area determines about two third of the chip area and the cell stability determines the soft error rate and the sensitivity of the memory to process tolerances and operating conditions [2].

Power consumption is one of the major concerns of VLSI circuit designs for which CMOS is the primary technology [3]. Hence, power consumption of the SRAM must be reduced. To achieve higher reliability and longer battery life for portable applications, low power cache is necessary. Since SRAM is used in cache memory. Shirked transistor sizes and reduced power supply voltages lead to lower noise margin. Due to these problems, devices more sensitive to noise sources [4]. This prevents the scaling of the conventional 6T SRAM bit-cell to lower supply voltages and to newer technology.

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SRAM designs thus becomes more challenging if we need low power, high performance fast responding SRAMs. Many newer circuitry having larger transistor count i.e. 7T, 8T, 9T, and 10T etc. has been implemented. This leads to larger power consumption. The probability of switching activity factor rises as the number of transistor increases and thus consumes larger space. The recent published works on dynamic feedback 8T SRAM [5] improves the write ability not the read stability.

The ultimate goal of this work is to improve the read stability and power consumption. Thus an alternate bit-cell that provides a better trade-off between area, performance, stability and power consumption. Our 10T SRAM bit cell is different from existing SRAM bit-cell topologies. The proposed 10T SRAM cell uses transmission gate and stacked transistor. The proposed SRAM does not require pre-charge circuit as required in prior 8T SRAM cell and sense amplifier circuit as required in 6T SRAM cell. Then we propose a 1-bit SRAM memory array using the proposed 10T SRAM bit cell which consumes less area than the conventional ones.

In this paper, we present a comprehensive comparison of the proposed 10T SRAM bit cell with the conventional 6T and 8T SRAM bit cell in terms of Read Static Noise Margin and power consumption. Then we again compare the proposed 1-bit memory array using the proposed 10T SRAM cell with the conventional 1-bit 6Tand 8T memory array in terms of power consumption and area.

The paper is organized as follows; in section 2 conventional 6T and 8T discussed, then their problems and the method to find Read Static Noise Margin are also discussed. In section 3 we discussed about the proposed 10T SRAM cell. In section 4, 1-bit memory array using the proposed memory cell, conventional 6T SRAM cell and Conventional 8T SRAM cells are discussed. In section 5 we present measured results. Finally, section 6 summarizes and concludes.

2. 6T AND 8T SRAM BIT CELL OVERVIEW

In this section we discussed the conventional 6T and 8T SRAM bit cells and the method to find Read Static Noise Margin is discussed. The problems with 6T and 8T SRAM cells are also discussed in this section.

2.1 CONVENTIONAL 6T SRAM CELL

The conventional 6T SRAM bit cell is shown in Fig.1. It consists of two cross coupled inverters with two pass transistors connected to complimentary bit-lines (BL and BLB). M1 and M2 are called drivers, M3 and i4 are called the load transistors and M5 and M6 are access transistors. The output nodes of inverters (M1 and M3) and (M2 and M4) are called *Q* and *QB* respectively. The gate of the pass transistors are connected to the Word Line (WL). SRAM cells perform three different operations read, write and hold operation [6].

The read operation is performed by activating WL and pre-charging the bit lines to higher voltages. The hold operation is performed by deactivating BL, BLB and WL. Assume that the cell is originally storing a "1" at node *Q*. If we wish to write a

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"0" then activate WL and then set BL to "0" and BLB is given"1". It is always not necessary to have two bit lines. The signal and its inverse are given to improve the noise margin. These bit lines carry the data from the memory cell to the sense amplifier.

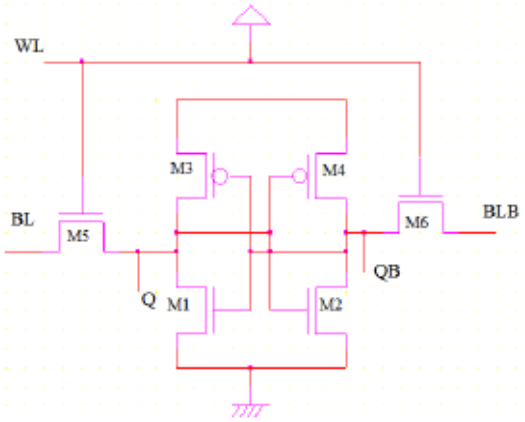

Fig.1. Conventional 6T SRAM cell

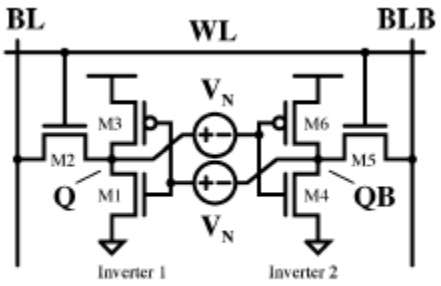

Fig.2. Standard set up for finding SNM [7]

In Fig.2 DC voltage VN sources are introduced at the internal nodes in the bit-cell. As DC voltage sources increases the stability of the cell changes [7]. The Fig.3 shows the most common way of representing the SNM graphically for a bit-cell holding and reading data. It plots the Voltage Transfer Characteristic (VTC) of inverter 2 and inverse VTC from inverter 1. The resulting is a two-lobbed curve called "a butterfly curve" and is used to determine the SNM. SNM is obtained by finding the length of the side of the largest square that can be embedded inside the lobes of the butterfly curve [2]. For the best way of understanding this concept, increase the value of VN from "0". This causes the VTC-1 for inverter 1 to move downward and VTC for inverter 2 to move towards right [7]. The curves meet at only two points once they are moved by the SNM value. The stability of the SRAM cell mainly depends up on the static noise margin [2].

The stability of the SRAM during read operation i.e. Read Static Noise Margin (RSNM) can be obtained by activating word-line and pre-charging BL and BLB to higher voltage. The internal node representing a zero gets pulled upward through the access transistor. This is mainly due to the voltage dividing effect across the access transistor (M5 and M6) and driver transistor (M1 and M2). This increase in voltage degrades SNM during the read operation [7].

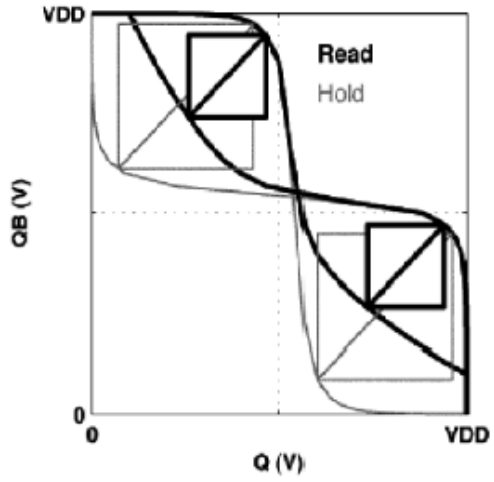

Fig.3. Example butterfly curve for SNM during hold and read operation [7]

PROBLEM WITH CONVENTIONAL 6T SRAM CELL

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The conventional 6T SRAM cell shown in Fig.1 is the most commonly used implementation having the advantage of very less area [8]. The cells are most vulnerable towards noise during the read and write operation and causes potential stability problem in the cell. So the cell structure must be designed properly for read margin and write margin.

During the read operation, a stored "0" can be overwritten by a "1" when the voltage at node reaches the threshold voltage of NMOS M1 to pull node Q down to "0" and in turn pull node QB up even further to "1" due to the mechanism of positive feedback arising in the structure. This causes wrong data being read or destructive read when the cell changes state [2].

To increase the RSNM, the potential of the gate electrode driver transistor made higher than that of the pass transistor so that the cell ratio becomes higher [8]. Cell ratio [9] is defined as the transistor strength ratio of the driver transistor to the access transistor. There are two techniques to implement such a relationship either suppress the word line voltage or boost the cell VDD level. If we suppress the word-line voltage, the cell current becomes too low to read at the lower VDD boundary due to the suppressed word-line and for the boosted cell VDD, higher power supply for the array cause excessive device reliability and power also increases. The Cell Ratio should exceed much since it increases the area of the SRAM memory cell.

Cell Ratio is very important parameter during the read operation. There is another parameter called pull up ratio which is mainly considered to achieve the write ability of the cell. Pull up Ratio (PR) is defined as the ratio of the size of the load transistor to the access transistor. So we cannot recommend this method in practical because increasing cell ratio results larger area and the power consumption also gets increased. SRAM cells must be designed properly; otherwise it may change its state during read and write operation [10].

CONVENTIONAL 8T SRAM CELL

The problem with conventional 6T SRAM cell can be overcome by using conventional 8T SRAM cell. The major advantage of 8T SRAM cell is that the data nodes are fully decoupled from read access and due to this the read stability of the cell is improved. Two NMOS transistors, along with extra read word-line and read-bit-line, are added to provide separate read port to the 8T SRAM cell which is shown in Fig.4. The word line for write is different from the word line read. The read operation is performed by pre-charging read bit line (RBL) to higher voltages and by activating read word line (RWL). Thus by doing this the read stability problem in conventional 6T SRAM cell is avoided and better read stability is retained in conventional 8T SRAM cell. The read stack and the use of short local bit lines, the 8T can provide high performance [4].

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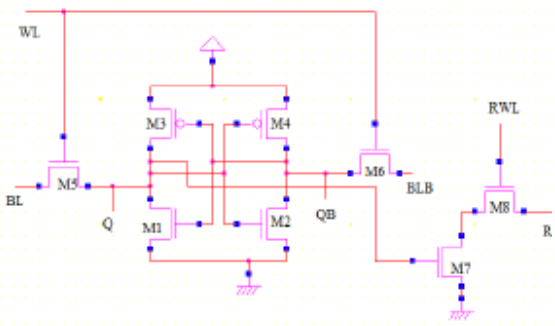

Fig.4. Conventional 8T SRAM cell

3. PROPOSED 10T SRAM CELL

In the proposed 10T SRAM cell, a transmission gate is used for read operation and also a pair of NMOS transistors is added in each of the pull down path. Thus the sub-threshold leakage current flowing through a stack of series connected transistors reduces when more than one transistor of the stack is turned off. This effect is known as the "stacking effect" [11].The leakage of a two transistor stack is in an order of magnitude less than the leakage in a single transistor. Thus the power consumption is reduced considerably due to the stacking effect. Both NMOS devices and PMOS devices exhibit poor performances when transmitting a particular logic. NMOS degrades the logic level "1" and PMOS degrades the logic level "0". Thus a perfect pass gate is constructed from the combination of NMOS and PMOS devices working in a complementary way, leading to improved switching performances. The proposed 10T SRAM cell is shown in Fig.5.

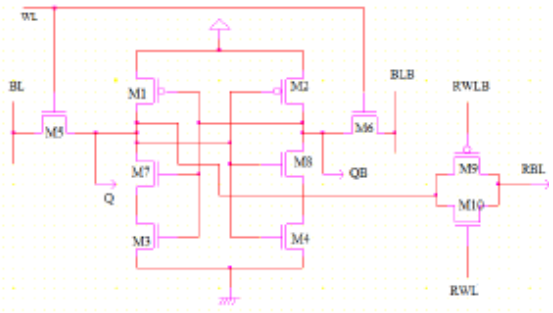

Fig.5. Proposed 10T SRAM cell

transistor M9 of the transmission gate. When RWL and RWLB are asserted, the transmission gate is ON; a stored node is connected to RBL. The value at node Q is being transferred or read through RBL. The advantage of this 10T SRAM cell is that it does not require a pre-charge circuit cells. Hence the stored value is passed directly through the transmission gate.

Charging/discharging power on the RBL is consumed only when RBL is changed. Consequently no power is dissipated on the RBL if an upcoming data is the same as the previous state. Thus the proposed design reduces the bit-line power in both cases that the consecutive "0" and consecutive "1" are read out. The read stability of the proposed design is higher than that of others due to the introduction of transmission gate power consumption is also reduced due to the introduction of stacking effect.

4. SRAM MEMORY SYSTEM FOR WRITING AND READING A SINGLE DATA BIT

In this paper the conventional 6T and 8T SRAM bit cells is being compared with the proposed design as shown in Fig.5 that enhances the data stability by improving the Read Static Noise Margin and also reduces the power consumption. Thus proposed 10T

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SRAM cell is being used for making an SRAM memory. For writing and reading a single data bit, there is a requirement of write driver, pre-charge circuit and sense amplifier in conventional 6T and 8T SRAM. One of the major advantages of this proposed design is that it does not necessary to prepare a pre-charge circuit and sense amplifier circuit in 6T and 8T SRAM cells because the stored node is directly passed through the transmission gate. The circuit for writing and reading a single data bit using the proposed 10T SRAM cell is shown in Fig.6.

The proposed circuit do not need sense amplifier and pre-charge circuit only write driver is used as peripheral circuit which considerably reduces the number of transistors which in turn reduces the area. Write Enable (WE) of the write driver is activated and then data is given into the data pin of the write driver. Write driver provide data and its compliment BL and BLB which is given to the proposed 10T SRAM cells BL and BLB pins. The data and its inverse will obtain at Q and QB. For reading
data, the transmission gate is turned ON by activating RWL and RWLB. Thus the stored data can be read through RBL. The schematic of conventional 6T, 8T is shown in Fig.7 and Fig.8. The conventional 6T and 8T SRAM cell has write driver, pre-charge circuit and sense amplifier for reading a single bit. Use of all these peripherals increases the power consumption.

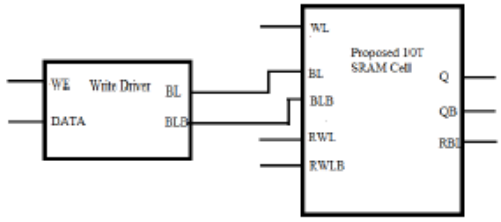

Fig.6. Block diagram of 10T SRAM cell for reading a single bit

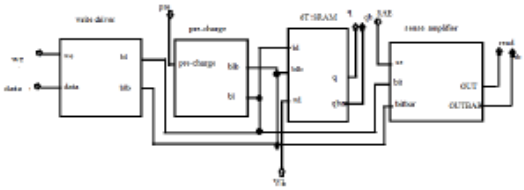

Fig.7. Schematic of 6T SRAM cell for reading a single bit

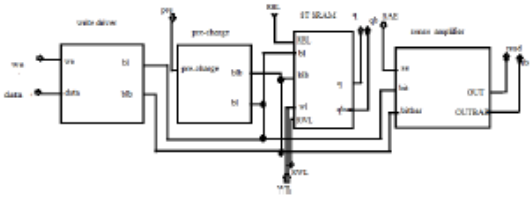

Fig.8. Schematic of 8T SRAM cell for reading a single bit

5. SIMULATION RESULTS AND DISCUSSION

Mentor Graphics ELDO Pyxis Schematic Editor is used for circuit design and the circuit is analyzed and verified the output using E-Z wave viewer for functionality through simulations. The target technology is TSMC 180nm CMOS process. Simulations are carried out for a supply voltage of 1.8V in order to prove that proposed design shows better performance for read SNM and power consumption.

POWER CONSUMPTION ANALYSIS

The existing and proposed bit cells and 1-bit memory array have been simulated for a supply voltage of 1.8V. The Table.2 shows that the power consumption of proposed 10T SRAM cell has less power consumption than the existing ones. From Table.3 we can see that the power consumption of proposed 1-bit memory array using the proposed has

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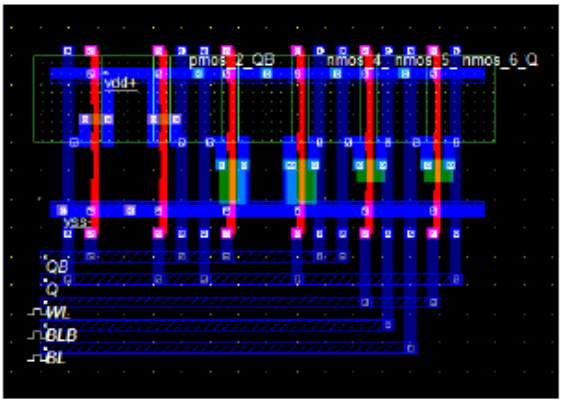
remarkably less power consumption compared to the existing 1-bit SRAM memory array using the 6T and 8T SRAM bit cells

Table.2. Power Consumption of different SRAM bit cells

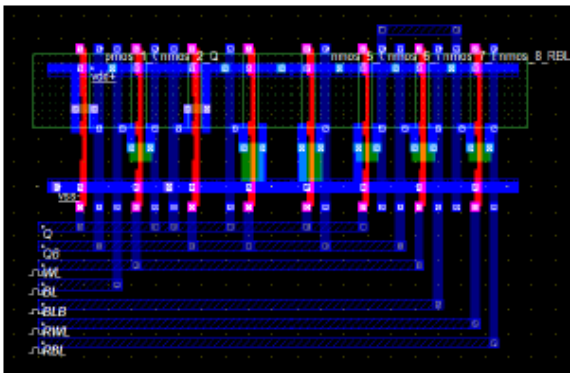
Technology	SRAM topology	Power Consumption (pW)
180nm	6T	40.9323
	8T	43.0151
	Proposed 10T	21.708

Table.3. Power consumption of different 1-bit memory array

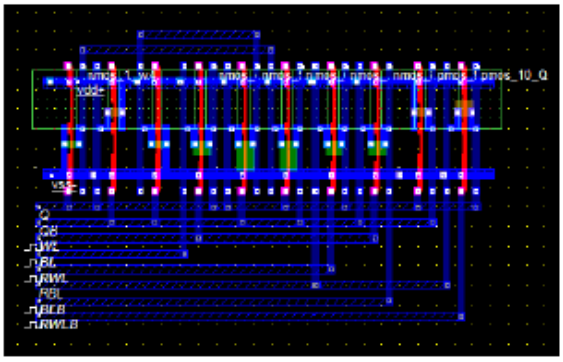
Technology	1-bit SRAM memory array	Power Consumption
180nm	6T	133.7634 µW
	8T	144.2718 µW
	Proposed 10T	75.8232 pW



Layout of 6T SRAM cell



Layout of 8T SRAM cell



Layout of proposed 10T SRAM cell

Table.4. Area analysis of different SRAM bit cells

SRAM cells	6T	8T	Proposed 10T
Area (μm^2)	28.1088	1.3934	1.8064

Table.5. Area analysis of peripheral circuits

Peripherals	Pre-charge Circuit	Write driver	Sense amplifier
Area (μm^2)	12.1196	76.032	28.8948

6. CONCLUSION

In this paper, we have presented a 1-bit 10T SRAM memory that provides better read stability, lower power consumption and lesser area compared to conventional 6T, conventional 8T 1-bit memory array. It also reduces the bit-line leakage problem in the conventional 8T SRAM cell and the read stability problem in conventional 6T SRAM cell. Thus the proposed 10T SRAM can be used as a cache memory in internal CPU and can be also used in industry and military purposes.

Measurements from an 180nm bulk CMOS confirm the successful operation of the proposed 1-bit 10T SRAM memory. To conclude, for technologies that are challenging in read stability, power and area, the proposed 1-bit 10T SRAM memory is an alternative bit-cell option due to its high read stability, lower power consumption and lesser area.

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