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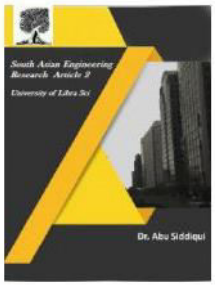

SURFACE ENGINEERING BASED REDUCTION OF THERMAL INTERFACE IMPEDANCE

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Abstract

The ever-increasing demand for more functionality of electronic and optoelectronic components led to increased packaging and thermal power densities. Higher processing density can be reached by developing thermal management solutions. The current technology in electronic packaging is to attach the die to heat spreader, using materials known as Thermal Interface Materials (TIM), such as solder or silver sinter pastes. The advantage of these materials is their relatively high thermal conductivity; however, there are major problems such as voiding and degradation of TIMs over time [1]. Furthermore, the thermal resistance of the interface between TIM and surfaces is considered as a serious issue in electronics packaging. In this work, we present a new scheme to reduce thermal impedance using surface patterning. Heat transfer enhancement in this method is based on increasing heat transfer surface area per unit die are and replacing TIM with patterns made of high thermal conductive materials such as Copper. Effect of different parameters such as pattern height, diameter and pitch on heat transfer rate was investigated both experimentally and numerically. Thermal resistance was measured using conventional 1-dimensional heat transfer setup. Finally, our experimental results show that using this scheme will increase effective thermal conductivity by almost 5-fold.

Keywords: Thermal Impedance, Thermal Interface Materials, surface patterning, surface engineering, Thermal Management

INTRODUCTION

Lighting Emitting Diodes (LEDs) are forming next generation of lighting due to their exceptional properties such as environmental friendly, low power consumption and long life. They are very reliable and they do not require much maintenance. Their small size makes them a good choice for many different lighting applications from Endoscopy in medical to home lighting applications. Available in

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many different colors, LEDs are a great option in visual indicators such as light signals. Thermal management is a crucial part in any LED luminaire design. It is shown that a good thermal management solution impacts on LED light out and life time [2]. Heat transfer path for an LED includes heat source,
interfaces, heat spreader and external cooling system. There have been a lot of studies carried out on how to design heat spreader and external heat exchangers and it is not the point of current study however, improving heat transfer at the surfaces have not been studied yet. Thermal Interface Materials (TIMs) are designed as one possible option to reduce interface thermal resistance between the mates. These materials are available in different forms such as adhesives, pastes and grease. A good TIM for LED application should have different properties such as high thermal conductivity, low thermal expansion mismatch respect to substrate, light reflection, reliability and low thermal degradation [3]. Most of current state of the art TIMs have disadvantage of thermal or light degradation after applying. Also voids formation is another disadvantage of most TIMs and many researchers have tried to discuss on void formation and how to reduce voids during assembly processes [4, 5]. The focus of this work is to reveal a new schematic that can be used to reduce interface thermal impedance using surface engineering and enhance heat transfer from the heat source.

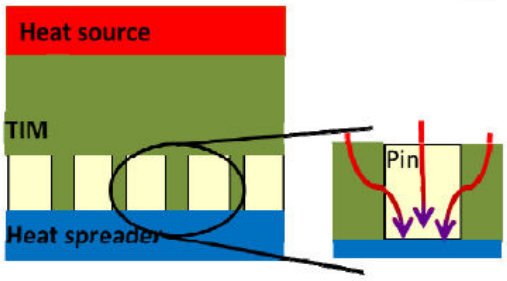

Fig. 1. Proposed scheme to reduce thermal impedance.

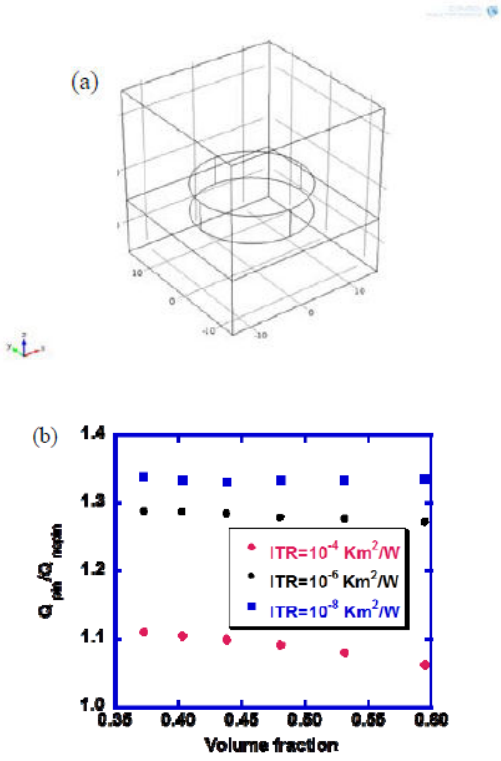

Fig. 2 (a) The geometry of the unit cell used in COMSOL simulation. Thermal resistivity will act everywhere that two materials are in contact such top and lateral side of the pillar and the rest of the flat surface. Predicted normalized heat transfer for a case when TIM and structure are both low thermal conductive (0.1 $Wm^{-1}K^{-1}$). Heat transfer surface area was kept constant for all the cases. Up to 33% enhancement is observed using surface patterning.

SIMULATION STUDY

To investigate our new approach, simulations were carried out using COMSOL Multiphysics. The aim of the simulations was to study if the patterning

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will enhance heat transfer. The main concern in using pillars to enhance heat transfer is the additional lateral surfaces that they introduce to the problem and therefore a concern for ITR effects. Hence it is important to explore the effect of interface thermal resistivity on the heat transfer enhancement. In order to study ITR effect for constant heat transfer surface area and different pillar's volume fraction, heat removal (Qpin) was calculated for patterned surface and then it was normalized by the amount heat removal from the flat surface (Qnopin). Furthermore, to highlight ITR effect, a case was simulated in which both TIM and pillars were set to be low thermal conductive material Wm-1K-1. Resistivity calculation for a no pattern case shows that a bond line thickness (BLT) of 20 µm o material with Wm-1K-1 has the thermal resistivity in the order of magnitude of 10-4 m2KW-1. Fig. 2 presents the normalized heat transfer after introducing pillars (pins) as a function of volume fraction of the structure. As Fig. 2 shows, heat transfer enhancement depends on the resistivity value. For low thermal resistivity of 10-8 m2KW-1 up to 33% enhancement can be achieved using surface patterning and this is only due to extended surfaces. For high resistivity value of 10-4 m2KW-1 the normalized heat transfer approaches to 1 which is expected because 10-4 m2KW-1 is the same resistivity as no-pin case. As shown in the Fig. 2 even for high thermal resistivity; patterning can improve heat removal. However the improvement is a function of volume fraction. Here, the volume fraction means the ratio of the volume of the pillars which are high thermal conductive (Cu) to the ratio of the TIM, with the BLT being the same as the height of the pillars. Volume fraction is a function of the pillar geometry. For instance if the pattern geometry is: pitch (p) = 40 µm, diameter (d) = 20 µm and height (h) = 24 µm; the volume fraction is obtained from:

$$volume\ fraction = \frac{\pi h d^2/4}{hp^2} = 0.196$$

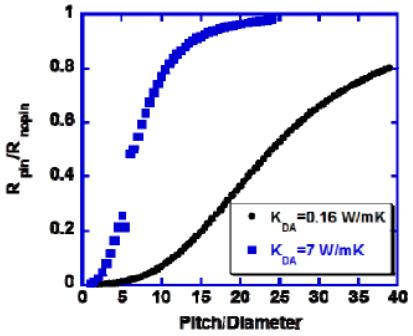

Fig. 3 Predicted normalized thermal resistance as a function of pitch/diameter for two different cases when TIM is 0.16 $Wm^{-1}K^{-1}$ and 7 $Wm^{-1}K^{-1}$. Pillar height is 24 µm and thermal resistivity is 10^{-5} m^2KW^{-1}. An optimum design can be defined based on the geometry and fabrication limitations. DA stands for Die Attach material.

As it is shown in Fig. 3, patterning is more beneficial when TIM has smaller thermal conductivity. Also an optimum design range of Pitch/Diameter ≥ 2 can be defined based on the fabrication limitations.

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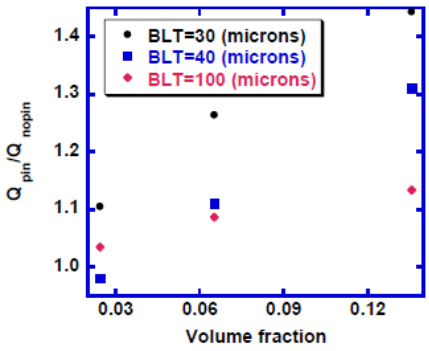

Fig. 4 Predicted results for the effect of the BLT on the heat transfer enhancement. Height and ITR are fixed but pitch varies.

EXPERIMENT

Based on the modeling results, reasons for heat transfer enhancement are extended heat transfer surface area per nit die area, and high bulk thermal conductive pillars embedded in TIM. Measurements were carried out using a modified ASTM D5470 method to measure effective thermal conductivity. As shown in Fig. 5 (a) a heater generates heat to the sample. This heater was insulated from top using a piece of Teflon so most heat goes to the samples. To find out heat loses a calibration procedure was carried out always with samples with known conductivity and it was found that heat loses trough convection is ~250 KW-1. The top surface is a 8mm x 8mm x 2mm Cu block. A hole also is manufactured in the Cu block. Two thermocouples were used to measure temperature at top and bottom of the sample. A piece of Al was used for heat sinking. Three samples with different thicknesses were fabricated and used for measurement. Each sample was measured three times to ensure the repeatability of the experiment. PDMS (Polydimethylsiloxane) was used as TIM for two reasons, 1- many TIMs are silicone based, 2- the rework ability of PDMS which allows us to un assemble the parts to look for voids. Calibration samples of sandwiched PDMS between two bare Copper pieces were also performed. Measurement results are presented in Fig. 5 (b). Thermal conductivity of 0.157 Wm-1K-1 was obtained for calibration PDMS samples, which is in good agreement with reported value in the data sheet (0.16 Wm-1K-1). Also for the pillars with diameter equals to 75 □m and pitch of 225 □m and height of 65 □m effective thermal conductivity of 1.09 Wm- 1K-1 was obtained. Uncertainty analysis was performed according to uncertainty propagation method. It was found that the error of the measured is less than 1%.

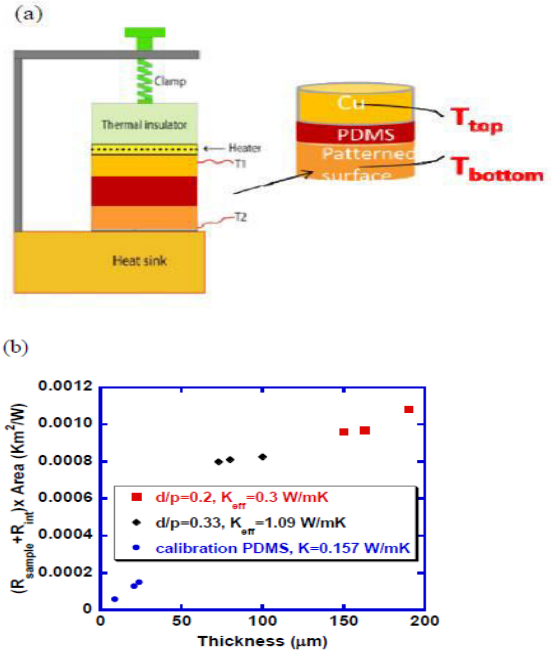

Fig. 5 (a) Schematic of the measurement setup. (b) Measurement results for the effective thermal conductivity for different pillar's structures. TIM was PDMS due to rework ability of this material.

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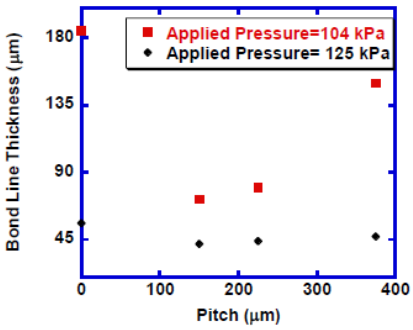

Fig. 6 Effect of patterning on the BLT for a pattern with 65 µm pillar's height. Pitch=0 µm is for the flat surface. Flat surface has the highest BLT. BLT decreases with increasing the pitch for the patterned surfaces.

This can be related to extra capillary forces that are introduced using pillars and help the flow to spread more uniformly. Furthermore, samples were un assembled to look for voids and no major void was observed in PDMS.

RESULTS AND DISCUSSION

The effect of patterning on the heat transfer enhancement was studied. Simulation results show that heat transfer enhancement is a function of interface thermal resistivity and volume fraction of the pillars. It was shown that to enhance heat transfer using patterning, the interface thermal resistivity should be the same or smaller than thermal resistivity of the TIM when it is squeezes between flat surfaces (Fig. 2). Otherwise the patterning would not enhance heat removal due to extra lateral surfaces and interface resistivity corresponds to those surfaces. Based on the same reason we predicted that if a TIM with lower thermal conductivity applied, more enhancement can be obtained from the patterning and results presented in Fig. 3 show this fact as well. Also based on Fig. 3 an optimum design region can be defined. Based on the fabrication limitations; we defined Pitch/Diameter should be equal or greater than 2. Finally, simulations show that to gain the maximum enhancement effect, BLT should be very close to the pillar's height. This criteria was used later to fabricate the samples for thermal measurements. A modified form of the ASTM D5470 was employed to carry out thermal measurements. PDMS (A type of silicone) was used as TIM since many TIMs are silicone based and also its rework ability. Our measurement shows up to 5 times enhancement in effective thermal conductivity of PDMS due to embedding high thermal conductive pillars (Cu) into PDMS. Furthermore, squeezing of PDMS between flat surface and patterned surface was studied and it was shown that BLT decreases for the patterned samples. This is basically due to the capillary forces that pillars introduce. This capillary force will help a more uniform flow on the chipand smaller BLT. It is important to mention that no major void was observed for the patterned samples however, for PDMS between flat surfaces, a big void at the center was always observed. Smaller BLT and less voids are another reasons that patterning may be effective to reduce thermal impedances.

CONCLUSION

A novel type of interface structure is proposed to reduce thermal impedances. Simulation and experiments were carried out and PDMS was used as TIM to proof of concept. More studies are required for the cases when TIM is filled with particles and

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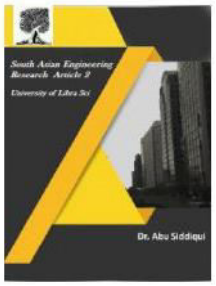

to extract the interface thermal resistance between TIM and patterned surface. It was shown that the effective thermal conductivity can be enhanced by a factor of 5 for current measurements.

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