2581-4575
International Journal For Recent Developments in Science & Technology
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A Multilevel Inverter Based on Switched Capacitor for High-Frequency Power Distribution System

V Vinay Kumar 1, Bhav Singh2

1 Assistant professor, Dept. of EEE, RGUKT Basar, Telangana-504107,India

2 Assistant professor, Dept. of EEE, RGUKT Basar, Telangana-504107,India

Abstract—The increase of transmission frequency reveals moremerits than low- or medium-frequency distribution among differ-ent kinds of power applications. High-frequency inverter serves as source side in high-frequency ac (HFAC) power distribution sys-tem (PDS). However, it is complicated to obtain a high-frequency inverter with both simple circuit topology and straightforward modulation strategy. A novel switched-capacitor-based cascaded multilevel inverter is proposed in this paper, which is constructed by a switched-capacitor frontend and H-Bridge backend. Through the conversion of series and parallel connections, the switched-capacitor frontend increases the number of voltage levels. The out-put harmonics and the component counter can be significantly reduced by the increasing number of voltage levels. A symmetrical triangular waveform modulation is proposed with a simple analog implementation and low modulation frequency comparing with traditional multicarrier modulation. The circuit topology, sym-metrical modulation, operation cycles, Fourier analysis, parame-ter determination, and topology enhancement are examined.

I INTRODUCTION

A traditional HFAC PDSis made up of a high-frequency (HF) inverter, an HF transmis-sion track, and numerous voltage-regulation modules (VRM). HF inverter accomplishes the power conversion to accommo-date the requirement of point of load (POL). In order to increase the power capacity, the most popular method is to connect the inverter output in series or in parallel. However, it is impracti-cal for HF inverter, because it is complicated to simultaneously synchronize both amplitude and phase with HF dynamics. Mul-tilevel inverter is an effective solution to increase power capacity without synchronization consideration, so the higher power ca-pacity is easy to be achieved by multilevel inverter with lower switch stress. Nonpolluted sinusoidal waveform with the lower total harmonic distortion (THD) is critically caused by long track distribution in HFAC PDS. The higher number of voltage levels can effectively decrease total harmonics content of stair-case output, thus significantly simplifying the filter design [7]. HF power distribution is applicable for small-scale and internal closed electrical network in electric vehicle (EV) due to mod-erate size of distribution network and effective weight reduc-tion [8]. The consideration of operation frequency has to make compromise between the ac inductance and resistance [9], so multilevel inverter with the output frequency of about 20 kHz is a feasible trial to serve as power source for HF EV application.

The traditional topologies of multilevel inverter mainly are diode-clamped and capacitor-clamped type [10], [11]. The for-mer uses diodes to clamp the voltage level, and the latter

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uses additional capacitors to clamp the voltage. The higher number of voltage levels can then be obtained; however, the circuit be-comes extremely complex in these two topologies. Another kind of multilevel inverter is cascaded H-Bridge constructed by the series connection of H-Bridges [12], [13]. The basic circuit is similar to the classical H-bridge DC–DC converter [14]. The cascaded structure increases the system reliability because of the same circuit cell, control structure and modulation. How-ever, the disadvantages confronted by cascaded structure are more switches and a number of inputs. In order to increase two voltage levels in staircase output, an H-Bridge constructed by four power switches and an individual input are needed. The-oretically, cascaded H-Bridge can obtain staircase output with any number of voltage levels, but it is inappropriate to the ap-plications of cost saving and input limitation.

Since the carrier fre-quency determines the switching frequency, a high switching loss is inevitable for the sake of high-frequency output. A boost multilevel inverter based in partial charging of SC can increase the number of voltage levels theoretically. However, the con-trol strategy is complicated to implement partial charging [20]. Therefore, it is a challenging task to present an SC-based multi-level inverter with high-frequency output, low-output harmon-ics, and high conversion efficiency [21].

Based on the study situation aforementioned, a novel multi-level inverter and simple modulation strategy are presented to serve as HF power source. The rest of this paper is organized as follows. The discussions of nine-level inverter are presented in Section II, including circuit topology, modulation strategy, operation cycle, and Fourier analysis. The parameter determi-nation and loss analysis are discussed in Section III. The further enhancement of 13-level inverter is studied in Section IV. The performance evaluation accomplished by simulation and experi-ment is described in Section V followed by concluding remarks.

SC-BASED CASCADED INVERTER WITH NINE-LEVEL OUTPUT

The proposed circuit is made up of the SC frontend and cascaded H-Bridge backend. If the numbers of voltage levels obtained by SC frontend and cascaded H-Bridge backend are $N_1$and N_2, respectively, the number of voltage levels is $2 \times N_1 \times N_2+1$ in the entire operation cycle.

A. Circuit Topology

Fig. 1 shows the circuit topology of nine-level inverter ($N_1 = 2$, $N_2 = 2$), where S_1, S_2, S_1, S_2 as the switching devices of SC circuits (SC1 and SC2) are used to convert the series or parallel connection of C_1 and C_2 . S_{1a}, S_{1b}, S_{1c}, S_{1d}, S_{2a}, S_{2b}, S_{2c}, S_{2d} are the switching devices of cascaded H-Bridge. V_{dc1} and V_{dc2} are input voltage. D_1 and D_2 are diodes to restrict the current direction. i_{out} and v_o are the output current and the output voltage, respectively.

It is worth noting that the backend circuit of the proposed inverter is cascaded H-Bridges in series connection. It is signifi-cant for H-Bridge to ensure the circuit conducting regardless of

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the directions of output voltage and current. In other words, H-Bridge has four conducting modes in the conditions of inductive and resistive load, i.e., forward conducting, reverse conducting, forward freewheeling, and reverse freewheeling.

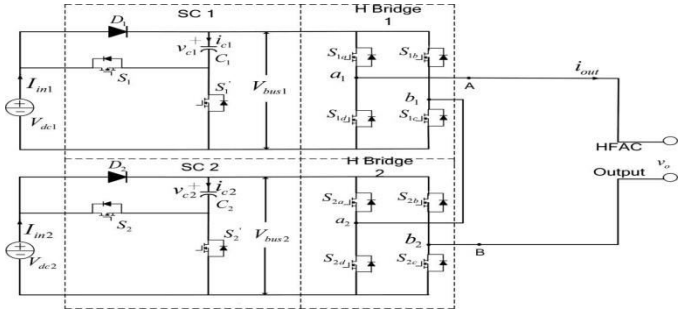

Fig Circuit topology of cascaded nine-level inverter ($N_1 = 2, N_2 = 2$).

B. Symmetrical Modulation

There are many modulation methods to regulate the mul-tilevel inverter, the popular modulations are the space vector modulation [22], the multicarrier PWM [23], and the selective harmonic elimination [24], [25], subharmonic pulsewidth mod-ulation [26], etc. However, most of them greatly increase the carrier frequency that is dozens times the frequency of refer-ence or output. A symmetrical phase-shift modulation (PSM) is introduced into the proposed multilevel inverter. The sym-metrical PSM ensures the output voltage of full bridge is sym-metrical to the carrier, so voltage levels can be superimposed symmetrically and carrier frequency is twice as that of the out-put frequency [27]. The structure of symmetrical PSM is shown in Fig. 2(a), and the operational waveform of symmetrical PSM is shown in Fig. 2(b).

The logic operations of gate signals are

gate 1 $= X\,OR\{Q(RS),\ Q(D)\}$

gate 2 $= X\,OR\{Q(RS),\ Q(D)\}$ (1)

gate 3 $= X\,OR\{AN\,D\{Q(RS),\ N\,OT\,(P\,W\,M\,)\},\ Q(D)\}$

gate 4 $= X\,OR\{AN\,D\{Q(RS),\ N\,OT\,(P\,W\,M\,)\},\ Q(D)\}.$

C. Operation Cycles

Fig. 3 demonstrates the ideal waveforms of proposed inverter. $V_c$is the triangular carrier, and$V_{p\,p}$is the peak value ofV_c. Themodulation signals of triangular carrier are V_{m1c},V_{m1b}, V_{m2c} and V_{m2b} . V_{m1b} and V_{m2b} are used to control phase-shift angles of H-Bridge 1 and H-Bridge 2, respectively, and δ_i is the duration of voltage levels controlled by them. V_{m1c} and $V_{m2c}$are used to control the alternative operations of SC1and SC2, respectively, and α_i is the duration of

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voltage levels controlled by them. Thus, the drive signals of H-Bridge switches (S_{1a}, S_{1b}, S_{1c}, S_{1d}, S_{2a}, S_{2b}, S_{2c}, S_{2d}) are phase-shifted pulse signals, while the drive signals of SC switches (S_1, S_2, S_1 , S_2) are complementary pulse signals. Two operational modes are presented as shown in Fig. 3(a) and (b). Mode 1 is similar to mode 2 apart from the different positions of modulation signals (V_{m1c} ,V_{m1b} , V_{m2c} , V_{m2b}). Consequently, the durations of each voltage level are controlled by modulation signals in both mode 1 and mode 2.

Active circuits of the operational mode 1 are demonstrated in Fig. 4. R_e is the equivalent load. When t satisfies $t_0 \leq t < t_1$in Fig. 3(a), the switches S_{1a} , S_{1b} , S_{2a} , $S_{2b}$are driven bythe gate-source voltage, respectively. H-Bridges 1 and 2 are in freewheeling state, and output voltage equals 0. Because S_1 and S_2 are on, the capacitors C_1 and C_2 are charged to V_{in}

($V_{d\,c1} = V_{d\,c2} = V_{\text{in}}$). The voltages on Bus 1 and Bus 2 are V_{in}as well.

When t satisfies $t_1 \leq t < t_2$ in Fig. 3(a), the switches S_{1a} , S_{1b} , S_{2a} , $S_{2c}$are driven by the gate-source voltage, respec-tively. H-Bridge 1 is in freewheeling state, and H-Bridge 2 is in positive conducting state. Output voltage equals V_{in} . Because $S_1$and $S_2$are on, the capacitors $C_1$and C_2keep charged to V_{in}($V_{d\,c1}$=$V_{d\,c2}$=V_{in}). The voltages on Bus 1 and Bus 2 areV_{in}as well. The current flow of this time interval is shown inFig. 4(b).

When t satisfies $t_2 \leq t < t_3$ in Fig. 3(a), the switches S_{1a} , S_{1c} , S_{2a} , $S_{2c}$are driven by the gate-source voltage, respec-tively. H-Bridges 1 and 2 are in positive conducting state. Output voltage equals $2V_{\text{in}}$. Because S_1 and S_2 are on, the capacitors $C_1$and C_2keep charged to V_{in}($V_{d\,c1}$=$V_{d\,c2}$=V_{in}). The volt-ages on Bus 1 and Bus 2 are V_{in} as well. The current flow of this time interval is shown in Fig. 4(c).

When t satisfies $t_3 \leq t < t_4$ in Fig. 3(a), the switches S_{1a} , S_{1c} , S_{2a} , $S_{2c}$are driven by the gate-source voltage, respec-tively. H-Bridges 1 and 2 are in positive conducting state. Output voltage equals $3V_{\text{in}}$. Because S_1 and S_2 are on, the capacitor C_1 keeps charged to V_{in} ($V_{d\,c1}$ = $V_{d\,c2}$ = V_{in}), and the capacitor C_2 is discharged. The voltages on Bus 1 and Bus 2 are V_{in} and $2V_{\text{in}}$, respectively. The current flow of this time interval is shown in Fig. 4(d).

III. DETERMINATION OF CAPACITANCE

As shown in Fig. 4, the capacitors are charged when they are in parallel with power source, and the capacitors are discharged when they are in series with power source. The switch S_i and S_i are driven alternatively during the half of output cycle. There-fore, the driven frequency of S_i and S_i is twice the frequency of output voltage, as well as the driven frequency of $S_{ia}-S_{id}$ is the same as the frequency of output voltage

The capacitance of C_i is determined by the voltage ripple of C_i that denotes the voltage fluctuation of multilevel output. The larger capacitance has the fewer ripple voltage. The voltage fluctuation over a narrow scope has a smaller power losses and higher capacitor

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2581-4575
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efficiency. The appropriated method of capac-itance calculation is that the maximum voltage ripple is 10% of the maximum capacitor voltage

It can be seen from the equations that the operational mode needs larger C_2 than that in operational mode 1. When the load is resistive, the phase of load current is agreed with the load voltage. The maximum discharging amount of capacitor is obtained in resistive load, because the peak load current is the midpoint of integration period. In other words, if the capacitance of C_i is derived in pure resistive load, it also maintains the less voltage ripples in inductive load.The peak current of the capacitor C_i is derived by Where VCi is the voltage on the capacitors Ci, VdF is the forward voltage drop of diode, rc is the equivalent series resistance(ESR) of the capacitors, ron is the internal on-state resistance of the switching device, and rd is the internal on-state resistance of the diode. Because of a small voltage difference of Vin and VCi , the peak current Ici is fewer for the larger Ci. Thus, the larger capacitor is needed to cut down undesirable peak current and prolong the capacitor lifetime. The analysis of switching loss is similar to the traditional cascaded H-bridge, while the capacitor losses consisting of ripple loss Prip and conduction loss Pcond are newly introduced by the proposed inverter. When the capacitor Ci is connected from series to parallel,the ripple is derived by the difference between the input voltage Vin and the capacitor voltage Vci . The voltage ripple of Ci iswhere VCi is the voltage on the capacitors Ci,VdF is the forward voltage drop of diode, rc is the equivalent series resistance (ESR) of the capacitors, ron is the internal on-state resistance of the switching device, and rd is the internal on-state resistance of the diode. Because of a small voltage difference of Vin and VCi ,the peak current Ici is fewer for the larger Ci. Thus, the larger capacitor is needed to cut down undesirable peak current and prolong the capacitor lifetime.

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FURTHER ENHANCEMENTS

The number of voltage levels can be further increased via two approaches. One is to increase the level number generated by SC circuit; the other one is to increase level number generated by cascaded H-Bridge. Thirteen-level inverters, as shown in Fig. 9, explain these two methods.

A 3 × 2 structure, as shown in Fig. 9(a), is derived by the enhancement of SC circuit, which needs 6 diodes, 4 capacitors, 14 switches, and 2 dc inputs. 2 × 3 structure as shown in Fig. 9(b) is derived by the enhancement of H-Bridge circuit, which needs 3 diodes, 3 capacitors, 18 switches, and 3 dc inputs. It can be found that 3 × 2 structure requires more diodes and capacitors than 2 × 3 structure. However, the number of power switches in 3 × 2 structure is less than that in 2 × 3 structure. Because the traditional cascaded H-bridge

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needs 24 switches and 6 inputs to produce 13 voltage levels, the numbers of power switches and inputs are greatly decreased by proposed inverter. In order to accomplish the staircase output with $4n + 1$ voltage levels, the component counts are compared in Table II.

TABLE II
COMPONENTS COMPARISON OF PROPOSED INVERTER AND CASCADED H-BRIDGE

Inverter type	Proposed inverter enhanced by SC n×2 topology	Proposed inverter enhanced by H-Bridge 2×n topology	Cascaded H-Bridge
Switching device	2n+8	6n	8n
Capacitor	2n-2	n	0
Diode	4n-6	n	0
DC bus	2	n	2n
Power losses	$(2n-2)loss_{cap}+(4n-6)loss_{diode}+(2n+8)loss_{switch}$	$nloss_{cap}+nloss_{diode}+6nloss_{switch}$	$8nloss_{switch}$

An $n\times$ 2 topology needs $2n - 2$ capacitors, $2n + 8$ switches, and 2 dc inputs; $2 \times n$ topology needs n capacitors, $6n$ switches, and n dc inputs. The traditional cascaded H-Bridge needs $8n$ switches and $2n$ dc inputs. With the same number of voltage levels, the proposed inverter needs less switching devices and inputs than the traditional cascaded H-Bridge. Considering the power losses, the traditional cascaded H-bridge has the higher switching losses caused by more switch devices. However, the proposed inverter newly introduces the capacitor loss that has already been examined in last section. Moreover, a flexible cir-cuit structure becomes possible. It is feasible for the proposed multilevel inverter to select suitable enhancement that can ac-commodate the requirements from different applications. For example, $2 \times n$ topology can be used for the power application sourced by multiple solar panels or batteries, and $n\times$ 2 topology can be used for the power application sourced by dual power sources.

CONCLUSION

In this paper, a novel SC-based cascaded multilevel inverter was proposed. Both 9-level and 13-level circuit topology are examined in depth. Compared with conventional cascaded mul-tilevel inverter, the proposed inverter can greatly decrease the number of switching devices. A single carrier modulation named by symmetrical PSM, was presented with the low switching frequency and simple implementation. The accordant results of simulation and experiment further confirm the feasibility of proposed circuit and modulation method.

Comparing with traditional cascade H-bridge, the number of voltage levels can be further increased by SC frontend. For instance, the number of voltage levels increases twice in half cycle of 9-level circuit, and the number of voltage levels in-creases three times in half cycle of 13-level circuit. With the exponential increase in the number of voltage levels, the har-

monics are significantly cut down in staircase output, which is particularly remarkable due to simple and flexible circuit topol-ogy. Meanwhile, the magnitude control can be accomplished by pulsewidth regulation of voltage level, so the proposed mul-tilevel inverter can serve as HF power source with controlled magnitude and fewer harmonics. This paper mainly analyzes nine-level and 13-level inverters. The method of analysis and design is also applicable to other members of the proposed in-verter.

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