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# A DIGITAL TIMING MISMATCH CALIBRATION TECHNIQUE FOR REAL-TIME ROTATION CALIBRATION IN SAR ADCS

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A digital calibration scheme is proposed to minimize the timing mismatch in time-interleaved analog-to-digital converters (TIADCs). First, the scheme is to subtract the outputs from adjacent channel ADCs and to utilize the expectations of the absolute value of the subtracted results to represent the actual sampling time interval. This brief presents an on-chip, real-time rotation calibration (RRC) technique aimed at alleviating the inter-channel offset mismatch in time-interleaved (TI) successive-approximation register analog-to-digital converter (SAR ADC). By leveraging auto-rotation calibration and self-compensation strategies in the analog domain, the proposed technique demonstrates robust performance across PVT variations. Two additional sub-channels are involved in the TI quantization mechanism, where the continuous rotation of the sampling clock distribution ensures their operation in calibration mode.

## 1. INTRODUCTION

Comparator is one of the fundamental building blocks in most analog-to-digital converters (ADCs). Many high-speed ADCs, such as flash ADCs, require high-speed, low power comparators with small chip area. High-speed comparators in ultra-deep sub micrometer (UDSM) CMOS technologies suffer from low supply voltages especially when considering the fact that threshold voltages of the devices have not been scaled at the same pace as the supply voltages of the modern CMOS processes [1]. Hence, designing high-speed comparators is more challenging when the supply voltage is smaller. In other words, in a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. Besides, low- voltage operation results in limited common-mode input range, which is important in many high-speed ADC architectures, such as flash ADCs.

Many techniques, such as supply boosting methods techniques employing body-driven transistors, current-mode design and those using dual-oxide processes, which can handle higher supply voltages have been developed to meet the low-voltage design challenges. Boosting and bootstrapping are two techniques based on augmenting the supply, reference, or clock voltage to address input-range and switching problems. These are effective techniques, but they introduce reliability issues especially in UDSM CMOS technologies. Body-driven technique adopted by Blalock, removes the threshold voltage requirement such that

body driven MOSFET operates as a depletion-type device. Based on this approach, in, a 1-bit quantizer for modulators is proposed. Despite the advantages, the body driven transistor suffers from smaller transconductance (equal to gmb of the transistor) compared to its gate-driven counterpart while special fabrication process, such as deep n-well is required to have both nMOS and pMOS transistors operate in the body-driven configuration.

Apart from technological modifications, developing new circuit structures which avoid stacking too many transistors between the supply rails is preferable for low-voltage operation, especially if they do not increase the circuit complexity. In, additional circuitry is added to the conventional dynamic comparator to enhance the comparator speed in low supply voltages. The proposed comparator of works down to a supply voltage of 0.5 V with a maximum clock frequency of 600 MHz and consumes 18 μW Despite the effectiveness of this approach, the effect of component mismatch in the additional circuitry on the performance of the comparator should be considered. The structure of double-tail dynamic comparator first proposed in is based on designing a separate input and cross coupled stage. This separation enables fast operation over a wide common-mode and supply voltage range.

A typical example is the SAR ADC. Conventionally, SAR ADCs were utilized for low speed, high-resolution ADCs due to their nature which requires multiple successive approximation (SA) cycles to complete the conversion. Typically, the number of required SA cycles is equivalent to the number of state bits. On the other hand, Pipelined and Flash ADC's conversion time is overwhelmingly short and have been adapted for high-speed applications. For example, in the case of Flash, the conversion delay is similar to that of a single comparator delay. The pipeline ADC's conversion delay consists only of a sub-ADC conversion and signal amplification, naturally suiting high-speed applications. However, all circuit blocks of the SAR ADC benefit from scaling and its performance have improved along with CMOS scaling. Due to that fact, the SAR ADC's performance improvement over the last decade was remarkable and looking back at the history of published SAR ADCs in the last two decades is very informative.

Although the SAR ADC has made a performance breakthrough in the past decade, the performance enhancement has hit a brick wall. We will study this further in this section. As a rule-of- thumb, realizing a high-resolution and high-speed SAR ADC is challenging. In this section, we will analyze some fundamental reasons behind this. One of the challenges which SAR ADCs face is the reference voltage settling constraints. Due to the structure of the binary C-DAC, when the large MSB capacitor is switched after the first comparison, a large amount of charging/discharging occurs. Such sudden charge actuation causes ringing in the reference voltage, because of the LC resonance of the bonding inductance. To obtain high accuracy by the SAR ADC, such voltage ringing must be attenuated within < LSB/2 to LSB/4, since actuated reference voltage corrupts the conversion accuracy.

Since a typical solution is to simply "wait" until the ringing calms down, this prolongs C-DAC and limits the conversion speed.

One way to reduce the voltage ringing is to utilize a large "decoupling" capacitor on-chip so that

sufficient amount of charge can be supplied on-chip. However, such decoupling capacitors can easily reach few nFs to achieve high-accuracy. Such capacitors can be even several times larger than the ADC core, and its cost overhead may not be acceptable for low-cost mobile SoC applications.

Another way to get around the voltage settling is by providing an on-chip voltage buffer. With a

sufficient buffer bandwidth, we can suppress reference voltage actuations. On the other hand, this breaks the premise that SAR ADCs do not require an active element; voltage buffers are a high-bandwidth power-hungry op amp. While the power consumption of the voltage buffer is typically excluded in the ADC performance presented at academic conferences, some works report that the utilized voltage buffer itself consumes more power than the SAR ADC itself

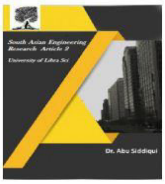
## 2. LITERATURE SURVEY

A 1.2-V Dynamic Bias Latch-Type Comparator in 65-nm CMOS With 0.4-mV Input Noise by H. S. Bindra, C. E. Lokin, D. Schinkel, A.-J. Annema, and B. Nauta

A latch-type comparator with a dynamic bias pre-amplifier is implemented in a 65-nm CMOS process. The dynamic bias with a tail capacitor is simple to implement and ensures that the pre-amplifier output nodes are only partially discharged to reduce the energy consumption. The comparator is analyzed and compared to its prior art in terms of energy consumption and input referred noise voltage. First-order equations are presented that show how to optimize the pre-amplifier for low noise and high gain. Both the dynamic bias comparator and the prior art are implemented on the same die and measurements show that the dynamic bias can reduce the average energy consumption by about a factor 2.5 for the same input-equivalent noise at an input common-mode level of half the supply voltage.

An 8-bit 150-MHz CMOS A/D converter by Y. T. Wang et al.,

This paper describes an 8-bit 5-stage pipelined and interleaved analog-to-digital converter that performs analog processing only by means of open-loop circuits such as differential pairs and source followers to achieve a high conversion rate. The concept of sliding interpolation is proposed to obviate the need for a large number of comparators or interstage digital-to-analog converters and residue amplifiers. The pipelining scheme incorporates distributed sampling between the stages so as to relax the linearity-speed tradeoffs in the sample-and-hold circuits, A clock edge reassignment technique is also introduced that suppresses timing mismatches in interleaved systems, and a punctured interpolation method is proposed that reduces the integral nonlinearity error with negligible speed or power penalty. Fabricated in a 0.6-/spl mu/m CMOS technology, the converter achieves differential and integral nonlinearities of 0.62 and 1.24 LSB, respectively, and a



signal-to-(noise+distortion) ratio of 43.7 dB at a sampling rate of 150 MHz. The circuit draws 395mW from a 3.3-V supply and occupies an area of 1.2/spl times/1.5 mm/sup 2/.

Analysis and Design of a Low-Voltage Low-Power Double-Tail Comparator by S. Babayan-Mashhadi and R. Lotfi

The need for ultra-low-power, area efficient, and high-speed analog-to-digital converters is pushing toward the use of dynamic regenerative comparators to maximize speed and power efficiency. In this paper, an analysis on the delay of the dynamic comparators will be presented and analytical expressions are derived. From the analytical expressions, designers can obtain an intuition about the main contributors to the comparator delay and fully explore the tradeoffs in dynamic comparator design. Based on the presented analysis, a new dynamic comparator is proposed, where the circuit of a conventional double-tail comparator is modified for low-power and fast operation even in small supply voltages. Without complicating the design and by adding few transistors, the positive feedback during the regeneration is strengthened, which results in remarkably reduced delay time. Post-layout simulation results in a 0.18- µm CMOS technology confirm the analysis results. It is shown that in the proposed dynamic comparator both the power consumption and delay time are significantly reduced. The maximum clock frequency of the proposed comparator can be increased to 2.5 and 1.1 GHz at supply voltages of 1.2 and 0.6 V, while consuming 1.4 mW and 153 µW, respectively. The standard deviation of the input-referred offset is 7.8 mV at 1.2 V supply.

A Low-Power High-Speed Comparator for Precise Applications by A. Khorami and M. Sharifkhani

A low-power comparator is presented. pMOS transistors are used at the input of the preamplifier

of the comparator as well as the latch stage. Both stages are controlled by a special local clock generator. At the evaluation phase, the latch is activated with a delay to achieve enough preamplification gain and avoid excess power consumption. Meanwhile, small cross-coupled transistors increase the preamplifier gain and decrease the input common mode of the latch to strongly turn on the pMOS transistors (at the latch input) and reduce the delay. Unlike the conventional comparator, the proposed structure let us set the optimum delay for preamplification and avoid excess power consumption. The speed and the power benefits of the comparator were verified using solid analytical derivations, process–VDD–temperature corners, and Monte Carlo simulations along with silicon measurements in 0.18 µm . The tests confirm that the proposed circuit reduces the power consumption by 50% and provides 30% better comparison speed at the same offset and almost the same noise budgets. Moreover, the comparator provides a rail-to-rail input Vcm range in fclk=500 MHz.

A Low-Power High-Precision Comparator with Time-Domain Bulk-Tuned Offset Cancellation by J. Lu and J. Holleman

A novel time-domain bulk-tuned offset cancellation technique is applied to a low-power high- precision dynamic comparator

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to reduce its input-referred offset with minimal additional power consumption and delay. The design has been fabricated in a commercially available 0.5-µm process. Measurement results of 10 circuits show a reduction of offset standard deviation from 5.415 mV to 50.57 µV, improved by a factor of 107.1. The offset cancellation scheme does not introduce observable offset or noise, and can achieve fast and robust convergence with a wide range of common mode input. On the other hand, there also exists an analog circuit whose performance improves by process scaling.

## 3. EXISTING METHOD

There are two types of comparators namely, Open-loop comparators and Regenerative or latch comparators. Open loop comparators are basically Op-amps without a feed-back whereas, regenerative comparators use positive feed-back mechanism to compare two signals. Many applications use Op-amp as an open-loop voltage comparator, but this method is generally not accurate and leads to slow performance. Hence the dynamic latch comparators used. It consists of an input pre-amplifier stage. At the reset phase (Clk=0) the output is pre-charged to logic "1". The output is evaluated at the regeneration phase (Clk=1).

There are three phases of operation, namely the reset phase, the amplification phase, and the

regeneration phase. In the reset phase (CLK = 0), the comparator is reset. In the amplification phase (CLK = 1), the input signal VIP–VIN is amplified and sent to the latch stage. In the regeneration phase, OUTP and OUTN regenerate to VDD or GND. As mentioned before, such a structure has the limitation of pMOS input pair in the latch stage.

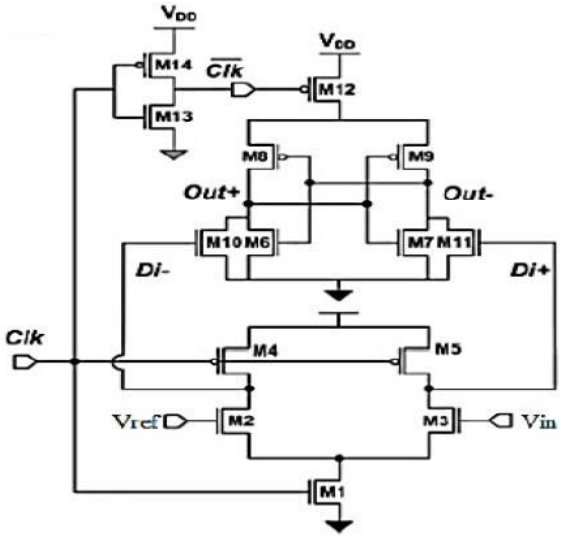


Fig 1 Circuit diagram of Conventional Double-tail Dynamic latch comparator

The Double-tail dynamic latch comparator is a comparator which has better performance at low voltage application. The Double-tail dynamic latch comparator has two discrete stages for input and for regenerative latch. Due to the separate stages, the comparator operates at a low voltage. Hence have stable offset voltage and increased speed [5]. Due to the presence of two tails one at the input stage and one at latch stage, the current is driven by two separate transistors. This is an advantage over the single tail comparators, in which the current is driven by single tail, and it requires high power The circuit diagram of conventional Double-tail dynamic latch comparator is shown in Figure 1. During the positive edge of the clock the tail transistors M1 and M12 are ON. M4 and M5 are OFF.

The output nodes are reset. During the negative edge of the clock the tail transistors M1 and M12 are OFF. Transistors M4 and M5 are ON. The nodes Di+ and Di- are

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charged to input voltages. Due to the arrangement of cross coupling inverters at latch stage positive feedback is produced and the output is evaluated.

Time-Interleaved Successive Approximation Register Analog-to-Digital Converters (TI-SAR ADCs) enhance sampling rates by operating multiple sub-ADCs in parallel. However, mismatches among these channels, particularly offset mismatches, can introduce spurious tones and degrade the overall performance of the ADC. Addressing these mismatches is crucial for maintaining signal integrity.

The Real-Time Rotation Calibration (RRC) technique is designed to mitigate inter-channel offset

mismatches in TI-SAR ADCs through an on-chip, real-time approach. This method employs auto- rotation calibration and self-compensation strategies within the analog domain, ensuring robust performance across variations in process, voltage, and temperature (PVT). The core of this technique involves two additional sub-channels that participate in the time-interleaved quantization process. By continuously rotating the sampling clock distribution, these sub-channels operate in calibration mode, allowing for the dynamic correction of offset mismatches without interrupting the ADC's normal operation.

## 4. PROPOSED METHOD

In order to reduce the kickback noise and further improve the speed, this brief proposes a modified version of comparator, Figure 2 shows the modified Double-tail dynamic latch comparator circuit diagram. The size of tail transistor Mtail1 is measured to have a low tail current through a differential input pair to achieve a longer integration time and a better gm / ID ratio for a large gain (less offset). The size of tail transistor Mtail2 is selected to have large tail current at the output stage for faster regeneration time.

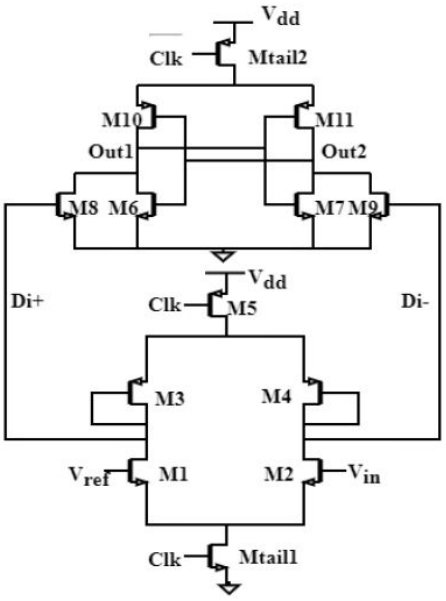


Fig 2. Circuit diagram of Modified Double-tail Dynamic latch comparator with kick-back noise

compensation

The two inverters are connected in cross-coupling format and provide a positive feedback and good shielding between input stage and output stage to reduce kick-back noise [3]. Diode connected transistors M3 and M4 were inserted between the input transistors. This reduces the output swing from Vdd to 0 to (Vdd - Vds) to 0. Hence reduces the dynamic power dissipation.

During the positive edge of the clock the tail transistors Mtail1 and Mtail2 are ON. Transistor M5 is OFF. The output nodes are reset to Vss. During the negative edge of the clock, tail transistors are OFF and Transistor M5 is ON. The nodes Di+ and Di- are

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charged to input voltages. The cross coupled inverter pair provides positive feed-back and the output is evaluated. This phase is called regeneration phase. The power is dissipated only in regeneration phase of the comparator which reduces the total power consumption. The input tail transistor M1is sized to have a small current driving capability. The tail transistor M13 at the latch stage is sized to have large current driving capability. The cross coupled inverter reduces offset voltage at the output. As an example, the proposed modified version is suitable for the time-interleaved noise-shaping SAR ADC in [13]. As pointed out in [13], its ADC speed is limited by the comparator speed, and its ADC resolution is limited by the comparator kickback noise. Although Zhuang et al. [13] use a channel isolation to reduce the influence of kickback noise, this isolation increases the complexity of system. By contrast, the proposed modified version of three-stage comparator can solve these issues. It has the fastest speed and the smallest kickback noise compared to other comparators.

## 5. RESULTS

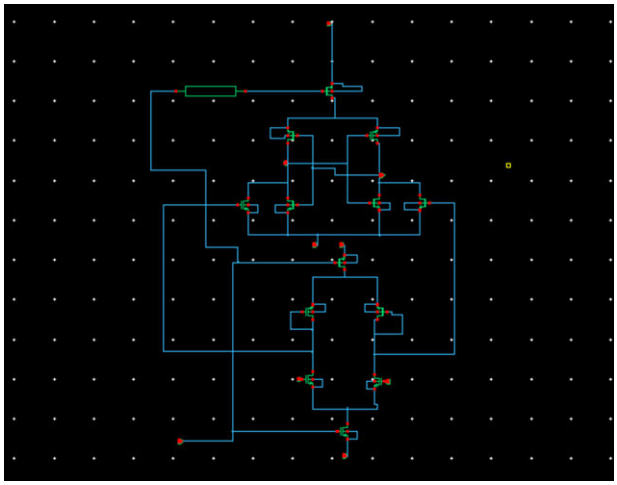

Fig 3 Circuit diagram of Modified Double-tail dynamic latch comparator

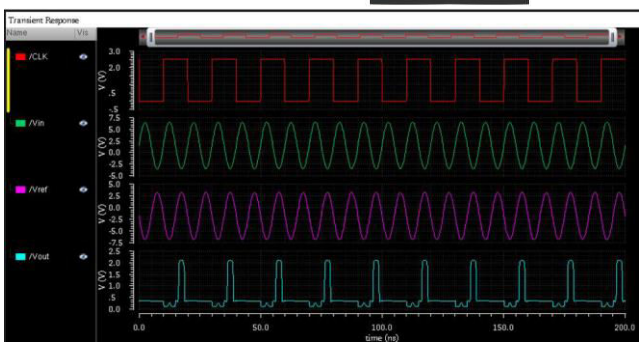


Fig 4 Waveforms of Modified Double-tail Dynamic latch comparator

| Sno. | Parameters | Existing System | Proposed System |
|---|---|---|---|
| 1. | Area | | |
| 2. | Total power | 1.998352 mW | 1.611536 mW |
| 3. | Delay | 860.733 ms | 759.928 ms |
| 4. | Architecture | 8xTI | 8xTI |
| 5. | Technology | 90nm | 90nm |

Table 1: Parameters Comparison of Existing and Proposed System

## 6. CONCLUSION

Various types of Dynamic Latch Comparators were simulated using 180 nm CMOS technology in the Cadence Virtuoso environment to evaluate their performance in terms of power consumption, speed, and reliability. Among these, the modified Double-Tail Dynamic Latch Comparator exhibited superior characteristics, particularly in terms of power efficiency and operational stability. Notably, the modified design effectively eliminates glitches at intermediate nodes, ensuring reliable switching behavior. One of the key findings is that the modified comparator consumes only 1.611536mW, which is significantly lower than the power dissipated by conventional comparators. Despite having a higher transistor count, the design achieves a

notable reduction in delay, making it a compelling choice for applications requiring both high speed and low power consumption.

Additionally, the modified comparator addresses critical design challenges by offering low kickback noise, reduced input-referred offset, and minimal noise interference, enhancing its robustness and precision. These attributes make it particularly well-suited for high-speed, high-resolution Successive Approximation Register (SAR) Analog-to-Digital Converters (ADCs), where performance trade-offs between speed, power, and accuracy are crucial. Finally, measured results validate the effectiveness of the proposed comparators, confirming their suitability for low-power, high-performance applications in modern mixed-signal and digital circuits.

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