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LOW POWER LOW AREA EFFICIENT DESIGN FOR FIXED-WIDTH ADDER-TREE

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ABSTRACT:

Low-power, area-efficient and high-performance computing systems are increasingly used in portable and mobile devices. For such applications, digital signal processing (DSP) algorithms are implemented in fixed-point VLSI systems. Adder-tree (AT) commonly used in parallel designs of inner product computation and matrix-vector multiplication Approximate computing can decrease the design complication with an increase in performance and power efficiency for error tolerant applications like multimedia signal processing and data mining which can tolerate error, exact computing units is not always necessary. They can be replaced with their approximate counterparts. A new design approach for approximation of multipliers based on partial products is altered to introduce varying probability terms. Logic complexity of approximation is usually varied for the accumulation of modified partial products. Adders and multipliers form the key components in these applications. In Existing system, Implementation of multiplier comprises three steps generation of partial products, partial products reduction tree, and vector merge addition to produce final product from the sum and carry rows generated from the reduction tree. Second step consumes more power. To reduce power and improve approximate difference, a novel compressor based approximate adder is proposed. Approximate compressor is proposed to further increase performance as well as reducing the error rate.

1. INTRODUCTION

The rapid growth of portable and wireless computing systems in recent years drives the need for ultralow power systems. To lower the power dissipation, supply voltage scaling is widely used as an effective low-power technique since the power consumption in CMOS circuits is proportional to the square of supply voltage However, noise interference problems have raised difficulty to design the reliable and efficient microelectronics systems; hence, the design techniques to enhance noise tolerance have been widely developed . An aggressive low-power technique, referred to as voltage over scaling (VOS), was proposed in to lower supply voltage beyond critical supply voltage without sacrificing the throughput. However, VOS leads to severe degradation in signal-to-noise ratio (SNR). A novel algorithmic noise tolerant (ANT) technique combined VOS main block with reduced-precision replica (RPR), which combats soft errors effectively while achieving significant energy saving .Some ANT deformation

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designs are presented and the ANT design concept is further extended to system level.
However, the RPR designs in the ANT designs are designed in a customized manner, which are not easily adopted and repeated. The RPR designs in the ANT designs can operate in a very fast manner, but their hardware complexity is too complex. As a result, the RPR design in the ANT design of is still the most popular design because of its simplicity. However, adopting with RPR in should still pay extra area overhead and power consumption.
In this paper, we further proposed an easy way using the fixed-width RPR to replace the full-width RPR block Using the fixed-width RPR, the computation error can be corrected with lower power consumption and lower area overhead. In order not to increase the critical path delay, we restrict the compensation circuit in RPR must not be located in the critical path.

2.LITERATURE SURVEY:

IMPrecise adders for low-power Approximate CompuTing by Vaibhav Gupta, DebabrataMohapatra, Sang Phill Park, AnandRaghunathan and KaushikRoy:Low-power is an imperative requirement for portable multimedia devices employing various signal processing algorithms and architectures. In most multimedia applications, the final output is interpreted by human senses, which are not perfect

Energy-efficient signal processing via algorithmic noise-tolerance, by R. Hegde ; N.R. Shanbhag: In this a framework for low-energy digital signal processing (DSP) where the supply voltage is scaled beyond the critical voltage required to match the critical path delay to the throughputDesign of low-power high-speed truncation-error-tolerant adder and its application in digital signal processing,by N. Zhu, W. L. Goh, W. Zhang, K. S. Yeo, and Z. H. Kong: In modern VLSI technology, the occurrence of all kinds of errors has become inevitable. By adopting an emerging concept in VLSI design and test, error tolerance (ET), a novel error-tolerant adder (ETA) is proposed

Inexact designs for approximate low power addition by cell replacement, by H. A. F. Almurib, T. N. Kumar, and F. Lombard:,It has three designs of an inexact adder cell for approximate computing. These cells require a substantially smaller number of transistors compared to an exact full adder cell as well as known inexact designs Accuracy-configurable adder for approximate arithmetic designs by A. B. Kahng and S. Kang Approximation can increase performance or reduce power consumption with a simplified or inaccurate circuit in application contexts where strict requirements are relaxed.

A low-power, high-performance approximate multiplier with configurable partial error recovery by Cong Liu ; Jie Han ; FabrizioLombard;Approximate circuits have been considered for error-tolerant applications that can tolerate some loss of accuracy with improved performance and energy efficiency. Multipliers are key arithmetic circuits in many such applications such as digital signal processing (DSP). In this a novel approximate multiplier with a lower power consumption and a shorter

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critical path than traditional multipliers is proposed for high-performance DSP applications

3.EXISTING SYSTEM:

LOW-power, area-efficient and high-performance computing systems are increasingly used in portable and mobile devices. For such applications, digital signal processing (DSP) algorithms are implemented in fixed-point VLSI systems. Adder-tree (AT) commonly used in parallel designs of inner product computation and matrix-vector multiplication. Multiplier design also involves a shift-adder-tree (SAT) for accumulation of partial product bits. Word-length growth is a common problem encountered when multiplication and addition are performed in fixed-point arithmetic. The shape of the bit matrix of SAT is different from the AT. Consequently, word length grows in a different order in SAT and AT. Besides, there are few other bits also added in the SAT to take care of negative partial products of multiplier. Specific designs have been suggested for efficient realization of fixed-width multipliers with less truncation error. However, the scheme used in fixed-width multiplier is not appropriate to develop a fixed-width AT design due to different shaped bit-matrix. The full-width AT (FL-AT) design produces (w + p)-bit output for every N-point input-vector, where p = log2 N. For the same size input-vector, the fixed-width AT (FX-AT) design produces w-bit output. Conventionally, FX-AT design is obtained from the FL-AT design by employing direct or post-truncation. In direct-truncation (DT), one lower orderbit of each adder output of FL-AT is post-truncated, and in case post-truncation, {p} lower order-bits of final adder output of FL-AT are truncated. In recent years, several schemes have been suggested for approximate computation of addition using ripple carry adder (RCA) to save critical path delay (CPD) and area. The bio-inspired lower part OR adder is proposed based on approximate logic. Four different types of approximate adder designs are proposed. An approximate 2-bit adder is proposed in for approximate computation of triple multiplicand without carry propagation. These approximate designs can be used to implement RCA with less delay and area with some loss of accuracy. The approximate RCA design can be used to obtain fixed-width AT employing post-truncation. However, the approximate fixed width AT (APX-FX-AT) does not offer an area-delay efficient design.

Bit-level optimization of FL-AT for multiple constant multiplication (MCM) is proposed to take advantage of shifting operation. An efficient FL-AT design is proposed using the approximate adder of for imprecise realization of Gaussian filter for image processing applications. We find that the optimized AT of is specific to MCM based design and none of the existing design discusses the issues related to fixed-width implementation of AT. It is observed that direct truncation and post-truncation methods does not provide an efficient FX-AT design. It is necessary to have a different approach for developing efficient FX-AT design which is currently missing in the literature. An efficient FX-AT design

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certainly help to improve the efficiency of dedicated VLSI systems implementing complex DSP algorithm.

4. PROPOSED SYSTEM

The Adder plays a vital role in many applications of VLSI design. The Adder-tree (AT) commonly used in parallel designs of inner product computation and matrix-vector multiplication. Conventionally, fixed-width adder-tree (AT) design is obtained from the full-width AT design by employing direct or post-truncation. But, both of these methods are not provide a efficient design for adder tree. This paper proposes the novel design implementation in order to obtain the fixed width adder Tree design using the truncated input. The truncation error is compensated by the bias estimation formula which is based on the probabilistic approach. Based on the proposed scheme, three separate fixed width Adder tree includes the vector sizes of 8, 16 and 32 are designed. Thus, the proposed fixed width adder tree design for input vector sizes 8, 16 and 32 offers the better area delay product (ADP) and also has a better efficiency when compared to the existing fixed-width adder tree.

This is the most critical portion of design since it determines the speed, accuracy and powerconsumption. It consist of two parts, namely Carry Free Addition Block (CFAB) and ControlBlock (CB). The schematic of modified OR block is shown in Fig.1. In proposed modified ORblock-1 two more transistor are used whose input depends on CTL signal, where CTL signal is a control signal coming out from Control Block (CB). When CTL = 0, Ml is on and M2 is offleaving the OR block circuit to operate in normal OR operation mode. When CTL=1, Ml is OFF and M2 is ON, hence the output sets to ' 1 ' by connecting output node to VDD. Problem withproposed block in Fig. 2 is presence of NMOS as a pass transistor in output node i.e. weknows that NMOS is poor in passing strong logic '1', so, we will get degraded value of outputwhile connecting to VDD. To solve the problem of passing strong logic ' 1' we have proposed another modified OR block-2 by replacing NMOS with PMOS and rearranging the connection oftransistors as shown in Fig. 2

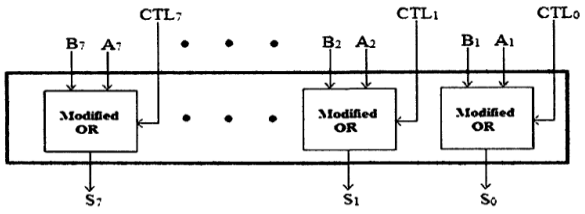

Fig.1 Block diagram

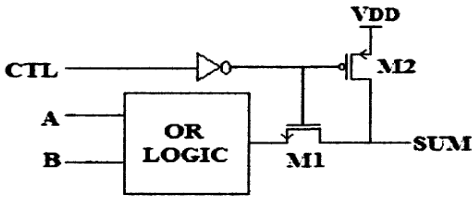

Fig.2 Modified OR Logic

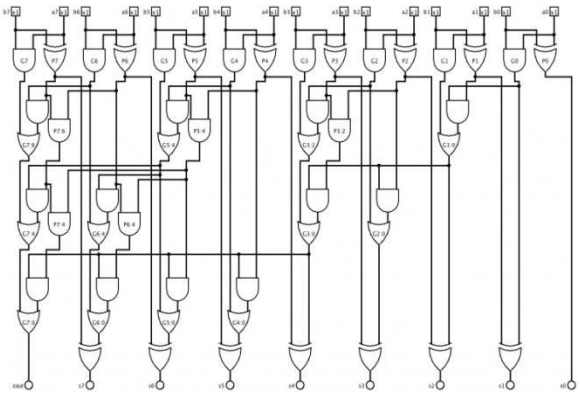

Fig.3 16-bit Fixed width adder tree

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5.RESULTS ANALYSIS

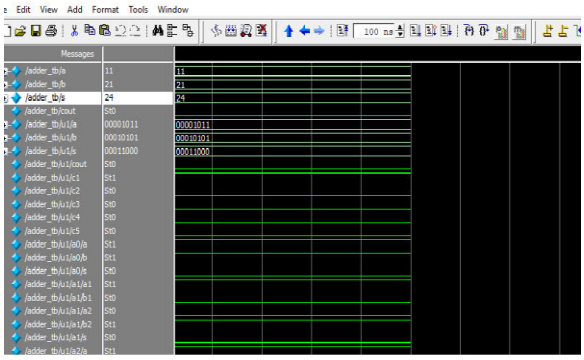

Fig.1 Simulation results

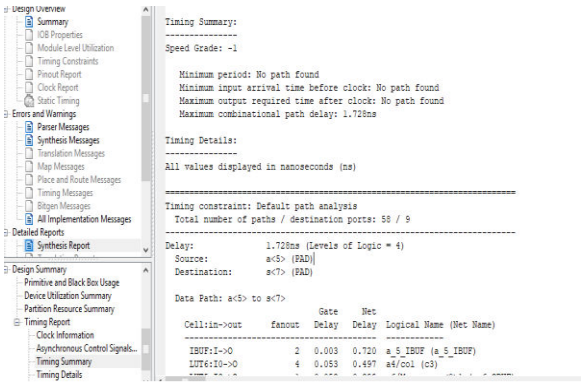

Fig.2 Synthesis report (Delay)

Fig.3 Power Analysis

PARAMETER	EXISTING METHOD	PROPOSED METHOD
DELAY	2.808ns	1.72ns
AREA	12 LUT's	10 LUT's
POWER	3.685	3.609

Table.1 Comparison Table

Table 1 shows the power and delaycomparison of the proposed adder with other adder designs. It is also shown from the table that the proposed designed is better in terms ofpower and delay.

5CONCLUSION & FUTURE SCOPE

Both measured and simulation results from this study have shown that fixed adders are not as effective as the simple ripple-carry adder at low to moderate bit widths. This is not unexpected as the Xilinx FPGA has a fast carry chain which optimizes the performance of the ripple carry adder. However, contrary to other studies, these adders have sindications that the carry-tree adders eventually surpass the performance of the linear adder designs at high bit-widths, expected to be in the 128 to 256 bit range. This is important for large adders used in precision arithmetic and cryptographic applications where the addition of numbers on the order of a thousand bits is not uncommon. Because the adder is often the critical element which determines to a large part the cycle time and power dissipation for many digital signal processing and cryptographical implementations, it would be worthwhile for future FPGA designs to include an optimized carry path to enable tree-based adder designs to be optimized for place and routing. This would improve their

performance similar to what is found for the RCA and also plan to explore possible FPGA architectures that could implement a "fast-tree chain" and investigate the possible trade-offs involved. The built -in redundancy of the Fixed carry-tree structure and its implications for fault tolerance in FPGA designs is being studied. The testability and possible fault tolerant features of the spanning tree adder are also topics for future research.

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