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DESIGN AND PERFORMANCE ANALYSIS OF BUCK & BOOST BASED GRID CONNECTED PV INVERTER

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Abstract—A single phase grid connected transformer less photo voltaic (PV) inverter which can operate either in buck or in boost mode, and can extract maximum power simultaneously from two serially connected sub arrays while each of the sub array is facing different environmental conditions, is presented in this paper. As the inverter can operate in buck as well as in boost mode depending on the requirement, the constraint on the minimum number of serially connected solar PV modules that is required to form a sub array is greatly reduced. As a result power yield from each of the sub array increases when they are exposed to different environmental conditions. The topological configuration of the inverter and its control strategy are designed so that the high frequency components are not present in the common mode voltage thereby restricting the magnitude of the leakage current associated with the PV arrays within the specified limit. Further, high operating efficiency is achieved throughout its operating range. A detailed analysis of the system leading to the development of its mathematical model is carried out. The viability of the scheme is confirmed by performing detailed simulation studies. A 1.5 kW laboratory prototype is developed, and detailed experimental studies are carried out to corroborate the validity of the scheme.

Index Terms—Grid connection, Single phase, Transformer less, Buck & Boost based PV inverter, Maximum power point, Mismatched environmental condition, Series connected module.

1. INTRODUCTION

Photovoltaic modules are connected in series and parallel in order to match the requirements regarding DC voltage and current of the inverter input [1]. The total DC power in such network is, however lower than the sum of the individual rated power of each module. The main reasons are static mismatch, environmental stress and shadow problems. The first aspect is related to manufacturing tolerances and aging of the module connected in the array. The second aspect instead refers to the effect of module defects due to weather conditions [2] [12]. Dynamic mismatches occurs when the modules operates far from its maximum power point. The PV modules connected in parallel or in series can not operate in their individual maximum power point because the voltage (in case of parallel connection) or current (in case of series connection) is forced to be equal in all the modules of the string [3]. Solar PV arrays are susceptible to large amounts of energy losses, due to partial shading. Partial shading is caused by light barriers like trees, chimneys, roof obstructions, power lines, debris, dust and bird droppings. In addition, mismatching can also occur if the photovoltaic modules are installed in different orientation or tilt. When it comes to series connected strings, the current of the solar array is only as strong as the weakest

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performing panel and this can reduce the solar array efficiency significantly [10] [11]. The MPP mismatch caused by shading is the main subject of the present work. When part of the panel is shaded, the shaded cells will produce less current than the non-shaded cells. Since all cells are connected in series, the same amount of current must flow through every cell. The non-shaded cells will force the shaded cell to pass more current than its new short circuit current. The shaded cell operates in reverse bias region to match this condition and cause a power loss to the system. The product of the current and negative voltage gives the power dissipated by the shaded cells. This power is dissipated as heat and hence, causes 'hot spots'. The probability that some cells in module or some modules in the string are potentially able to deliver strongly different currents in operating conditions is very high [12] and can not be neglected.In order to address the problem arising out of MEC in a PV system, various solutions are reported in the literature. An exhaustive investigation of such techniques has been presented . Power extraction during MEC can be increased by choosing proper interconnection between PV modules or by tracking global maximum power point (MPP) of PV array by employing complex MPP tracking (MPPT) algorithm . However, these techniques are not effective for low power SPGCT PV system. Similarly, reconfiguration of the PV modules in a PV array by changing the electrical connection of PV modules is not effective for SPGCT PV system due to the considerable increment in component count and escalation in operating complexity. In order to extract maximum power from each PV module during MEC, attempts have been made to control each PV module in a PV array either by having a power electronic equalizer or by interfacing a dc to dc converter . Schemes utilizing power electronic equalizer require large component count thereby increasing the cost and operation complexity of the system. The scheme presented in uses generation control circuit (GCC) to operate each PV module at their respective MPP wherein the difference in power between each module is only processed through the GCC. Scheme presented in uses shunt current compensation of each module as well as series voltage compensation of each PV string in a PV array to enhance power yield during MEC. The schemes based on module integrated converter use dedicated dc to dc converter integrated with each PV module. However, the efficiency of the aforesaid schemes are low due to the involvement of large number of converter stages, and further in these schemes the component count is high and hence they face similar limitations as that of power electronic equalizer based scheme. Instead of ensuring MPP operation of each and every module, certain number of modules are connected in series to form a string and the so formed strings are then made to operate under MPP. Even then there is not much reduction in overall component count and control complexity .An effort has been made in this paper to divide the PV modules into two serially connected sub arrays and controlling each of the sub array by means of a buck and boost based inverter so that optimum power evacuation from the sub arrays is ascertained during MEC. This process of segregation of input PV array into two sub arrays reduces the number of series connected modules in a sub array almost by half compared to that of the schemes. The topological structure and control strategy of the proposed inverter ensure that the magnitude of leakage current associated with the PV arrays remains within the permissible limit. Further, the voltage stress across the active devices is reduced almost by half compared to that of the schemes, hence very high frequency operation without increasing the switching loss is ensured. High frequency operation also leads to the reduction in the size of

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the passive elements. As a result the operating efficiency of the proposed scheme is high. The measured peak efficiency and the European efficiency (ηeuro) of the proposed scheme is found to be 97.65% and 97.02% respectively.

The detailed operation of the proposed inverter with mathematical validation is explained in Section II. Afterwards the mathematical model of the proposed inverter has been derived in Section III followed by the philosophy of control strategy in Section IV. The criteria to select the values of the output filter components are presented in Section V. The proposed scheme is verified by performing extensive simulation studies and the simulated performance is presented in Section VI. A 1.5 kW laboratory prototype of the proposed inverter has been fabricated to carry out thorough experimental studies. The measured performances of the scheme which confirm its viability are presented in Section VII.

2. PROPOSED INVERTER AND ITS OPERATION

The schematic of the proposed Dual Buck & Boost based Inverter (DBBI) which is depicted in Fig. 1 is comprising of a dc to dc converter stage followed by an inverting stage. The dc to dc converter stage has two dc to dc converter segments, CONV1 and CONV2 to service the two sub arrays, P V1 and P V2 of the solar PV array. The segment, CONV1 is consisting of the self-commutated switches, S1 along with its anti-parallel body diode, D1, S3 along with its anti-parallel body diode, D3, the free wheeling diodes, Df1, Df3 and the filter inductors and capacitors, L1, Cf1, and Co1. Similarly, the segment, CONV2 is consisting of the self-commutated switches, S2 along with

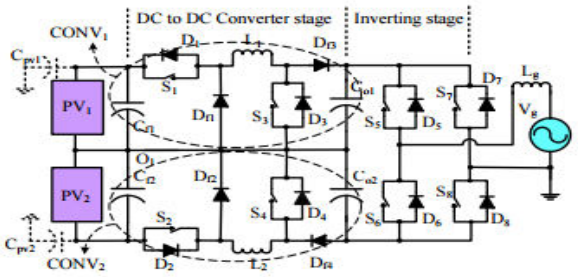

Fig. 1. Dual Buck & Boost based Inverter (DBBI)

its anti-parallel body diode, D2, S4 along with its anti-parallel body diode, D4, the free wheeling diodes, Df2, Df4 and the filter inductors and capacitors, L2, Cf2, and Co2. The inverting stage is consisting of the self-commutated switches, S5, S6, S7, S8, and their corresponding body diodes, D5, D6,D7 and D8 respectively. The inverter stage is interfaced with the grid through the filter inductor, Lg. The PV array to the ground parasitic capacitance is modeled by the two capacitors, Cpv1 and Cpv2.

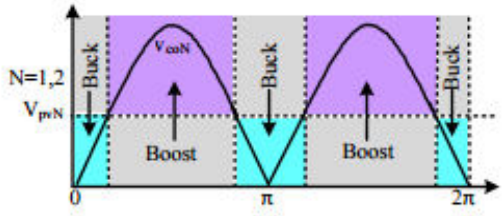

Fig. 2. Buck stage and Boost stage of the proposed inverter

Considering Fig. 2, CONV1 operates in buck mode when Vpv1 ≥ vco1, while CONV2 operates in buck mode when Vpv2 ≥ vco2. Vpv1, Vpv2 are the MPP voltages of P V1 and P V2 and vco1, vco2 are the output voltages of CONV1 and CONV2 respectively. During buck mode duty ratios of the switches, S1 and S2 are varied sinusoidally to ensure sinusoidal grid current (ig) while S3 and S4 are kept off. When Vpv1 < vco1, CONV1 operates in boost mode while CONV2 operates in boost mode when Vpv2 < vco2. During boost mode duty ratios of the switches, S3 and S4 are varied sinusoidally to ensure sinusoidal ig while S1 and S2 are kept on throughout this mode. The sinusoidal switching pulses of the switches of CONV1 and CONV2 are

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synchronized with the grid voltage, vg to accomplish unity power factor operation. The switches, S5 and S8 are kept on and switches S6 and S7 are kept off permanently during the entire positive half cycle (PHC) while during entire negative half cycle (NHC), the switches, S6 and S7 are kept on and switches, S5 and S8 are kept off permanently. All the operating states of the proposed inverter are depicted in Fig. 3.

When the isolation level and ambient temperature of sub array P V1 are different from that of P V2, the MPP parameters

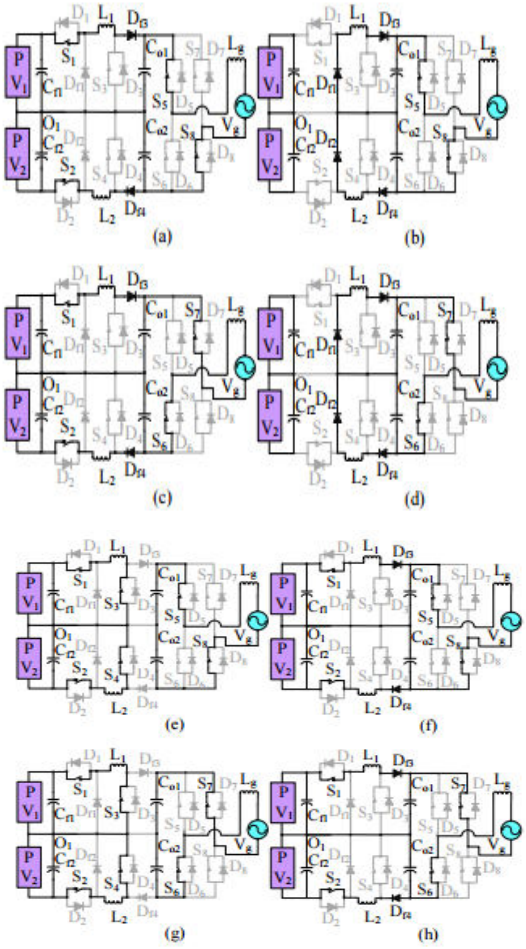

Fig. 3. Operating states of DBBI: (a) Active and (b) Freewheeling states in buck mode of PHC, (c) Active and (d) Freewheeling states in buck mode of NHC, (e) Active and (f) Freewheeling states in boost mode of PHC, (g) Active and (h) Freewheeling states in boost mode of NHC

of the two sub arrays, Vpv1 and Vpv2, MPP current, Ipv1 and Ipv2 correspond to P V1 and P V2 respectively and power at MPP, Ppv1 and Ppv2 correspond to P V1 and P V2 respectively differ from each other. By considering that both the sub arrays are operating at their respective MPP and neglecting the losses incurred in power processing stages, the average power involved with Co1 and Co2, Pco1 and Pco2 over a half cycle can be assumed equal to the power extracted from P V1 and P V2. Therefore,

$$P_{co1} = P_{pv1} \quad \& \quad P_{co2} = P_{pv2} \tag{1}$$

The power injected to the grid averaged over a half cycle, Pg can be written as

$$P_g = P_{pv1} + P_{pv2} \tag{2}$$

Further, at any half cycle

$$v_g = v_{co1} + v_{co2} \tag{3}$$

Hence, the instantaneous injected power to the grid, pg can be written as

$$p_g = v_g i_g = (v_{co1} + v_{co2}) i_g \tag{4}$$

Where in vco1 and vco2 denote the instantaneous quantities of Vco1 and Vco2 respectively. As ig is in-phase with vg,

$$I_g = \frac{P_g}{V_g} \tag{5}$$

Where in Vg and Ig denote rms values of vg and ig respectively. The power injected to the grid can be expressed as

$$\begin{aligned} P_g &= \frac{1}{\pi}\int_0^{\pi} p_g \, d(\omega t) \\ &= \frac{1}{\pi}\int_0^{\pi} v_{co1} i_g \, d(\omega t) + \frac{1}{\pi}\int_0^{\pi} v_{co2} i_g \, d(\omega t) \quad (6) \\ &= P_{co1} + P_{co2} \quad (7) \end{aligned}$$

As vco1 and vco2 are synchronized with vg. Hence

$$\begin{aligned} P_{co1} &= \frac{1}{\pi}\int_0^{\pi} V_{co1m} \sin(\omega t) \, I_{gm} \sin(\omega t) \, d(\omega t) \\ &= \frac{V_{co1m} I_{gm}}{2} \quad (8) \end{aligned}$$

Similarly,

$$P_{co2} = \frac{V_{co2m} I_{gm}}{2} \tag{9}$$

Where in the amplitudes of vco1, vco2 and ig are denoted as Vco1m, Vco2m and Igm respectively. Combining (1), (8) and (9)

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$$V_{co1m} = \frac{2P_{pv1}}{I_{gm}} = \frac{\sqrt{2}P_{pv1}}{I_g} = \frac{\sqrt{2}P_{pv1}}{P_g/V_g} \quad (10)$$

$$V_{co2m} = \frac{2P_{pv2}}{I_{gm}} = \frac{\sqrt{2}P_{pv2}}{I_g} = \frac{\sqrt{2}P_{pv2}}{P_g/V_g} \quad (11)$$

Similarly by combining (2), (10) and (11),

$$V_{co1m} = \frac{V_m P_{pv1}}{P_{pv1} + P_{pv2}} \quad \& \quad V_{co2m} = \frac{V_m P_{pv2}}{P_{pv1} + P_{pv2}} \quad (12)$$

The voltage templates of vco1 and vco2 appear as full wave rectified sinusoidal waveform with amplitudes, Vco1m and Vco2m respectively. Vm is the amplitude of vg. It can be deduced from (12) that the magnitudes of Vco1m and Vco2m are decided by the power extracted from each of the sub array. If the power extracted from P V1 is less than P V2, then Vco1m < Vco2m, whereas Vco2m < Vco1m if power extracted from P V2 is less than P V1. During buck mode, the duty ratios, d1 of S1 and d2 of S2 vary sinusoidally with an amplitude d1m and d2m, wherein

$$d_{1m} = \frac{V_{co1m}}{V_{pv1}} \quad \& \quad d_{2m} = \frac{V_{co2m}}{V_{pv2}} \quad (13)$$

while during boost mode the duty ratios, d3 of S3 and d4 of S4 vary sinusoidally with amplitude d3m and d4m, wherein

$$d_{3m} = 1 - \frac{V_{pv1}}{V_{co1m}} \quad \& \quad d_{4m} = 1 - \frac{V_{pv2}}{V_{co2m}} \quad (14)$$

The CONV1 and CONV2 are having the same output current ig. Hence, the input side currents before getting filtered by input filter capacitors of CONV1, isw1 and CONV2, isw2 can be related with ig in the buck mode by considering the switching cycle average of corresponding quantities as follows

$$\langle i_{sw1} \rangle_{T_s} = \langle d_1 \rangle_{T_s} \langle i_g \rangle_{T_s} \quad (15)$$

$$\langle i_{sw2} \rangle_{T_s} = \langle d_2 \rangle_{T_s} \langle i_g \rangle_{T_s} \quad (16)$$

Similarly by considering switching cycle average of corresponding quantities the relation between isw1, isw2 and ig can be deduced during boost mode as

$$\langle i_{sw1} \rangle_{T_s} = \langle \frac{1}{1-d_3} \rangle_{T_s} \langle i_g \rangle_{T_s} \quad (17)$$

$$\langle i_{sw2} \rangle_{T_s} = \langle \frac{1}{1-d_4} \rangle_{T_s} \langle i_g \rangle_{T_s} \quad (18)$$

Therefore, it can be inferred from (12) and (13) that if the isolation level of P V1 is lower than that of P V2, during buck mode, d1m < d2m, thereby hd1iTs < hd2iTs whereas during boost mode as per (12) and (14), d3m < d4m, thereby hd3iTs < hd4iTs . Hence, it can be concluded from (15), (16), (17) and (18) that in any operating mode, hisw1iTs < hisw2iTs , therefore Ipv1 < Ipv2. Following the same argument, Ipv1 > Ipv2 if the isolation level of P V1 is higher than that of P V2.

Considering Fig. 1 it can be noted that during operation in PHC, vcpv1 = vco2 + Vpv1, vcpv2 = vco2 − Vpv2 while during NHC vcpv1 = −vco1 + Vpv1, vcpv2 = −vco1 − Vpv2, wherein vcpv1 and vcpv2 are the voltages impressed across Cpv1 and Cpv2 respectively. Hence, the voltages across Cpv1 and Cpv2 contain significant amount of dc and low frequency components which also ensures that the magnitude of the leakage current is maintained within the limit specified in the standard, VDE 0126-1-1, and also cited in [23].

3. MISMATCH LOSSES

3.1 Static Mismatch

According to [1] the figure for static mismatch due to manufacturer's tolerance is below 1% for Si-based Modules. For thin film modules the manufacturing tolerances are generally higher. However, the fractional power loss due to manufacturing tolerances is about 2% [2]. Furthermore the effect of aging is investigated. Considering aging the mismatch losses may rise up to 12% in series strings. The studies make clear that the losses may be reduced drastically by means of an appropriate series parallel connections and a preselection of the modules. Thus the expected mismatch even in consideration of aging effects is in the range of 0.4 to 2.4%.

3.2. Dynamic Mismatch

3.2.1 without Bypass Diodes

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I-V curve of the PV module is affected decisively when solar cells are irradiated at different levels. It is already well known that the energy output decreases dramatically without bypass diodes compared to the lost total irradiation. In order to demonstrate this, the module in which all the 36 solar cells are series connected without bypass diodes and out of which one cell is partially shaded to different levels is simulated. Resultant characteristics of the whole module in partial shading have to be obtained. For this, as the solar cells are connected in series, for the given current the voltage has to be calculated by adding the corresponding voltage of shaded cell and non-shaded 35 cells. The shaded solar cell has significantly narrowed the current path in the module

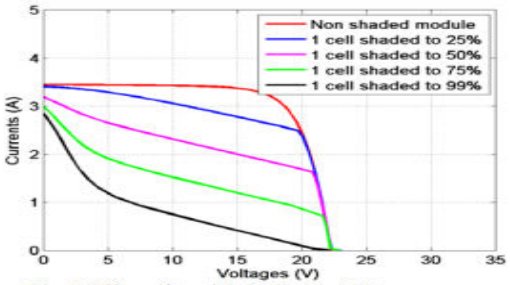


Fig. 4 Effect of partial shading in I-V curves

The partial shading is very dangerous for solar modules as a single cell shading out of 36 or 72 cells module can reduce most of the power output drastically. The shaded cell acts as load, dissipating power on itself which may lead to hot spot conditions and ultimately damages the cells. It is found that with the increase of percentage of single cell shading, mismatch losses increases. When single cell is shaded to 99% (100% shading is not possible because of diffused irradiation) the reduction in irradiance falling on the module is less than 3% but maximum power output in watts is reduced by more than 86%.

In the real world situations more complex shading situation than this can occur and lead to much higher mismatch losses. Further, different number of solar cells shading situation are simulated as shown in fig 5. It has been observed that the power loss because of partial shading is not proportional to the shaded area in the module as it was expected before. As seen in fig 5, with the increase in number of shaded cells, the effect in I-V characteristics is almost constant.

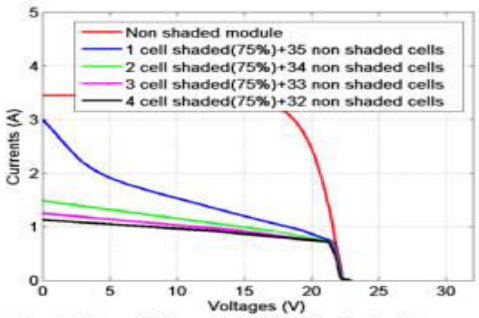
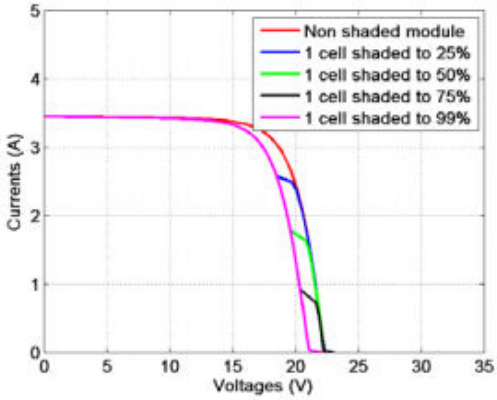


Fig.5 Effect of different number of cells shading

3.2.2 Bypass Diodes

To prevent shadowed cells from narrowing the current path in a string, and downgrading the performance of other cells in series and reducing the power production of the whole string , bypass diodes are usually placed in anti parallel (reverse biased) to small group of series connected cells(normally 18 or 24 cells). Module manufacturers employ bypass diodes to preserve array voltage and to minimize hot spot heating and the potential for cell failure when shaded [7]. For very sophisticated application (example: space applications), bypass diode are used across each cell. However in practice this is avoided because of the cost.



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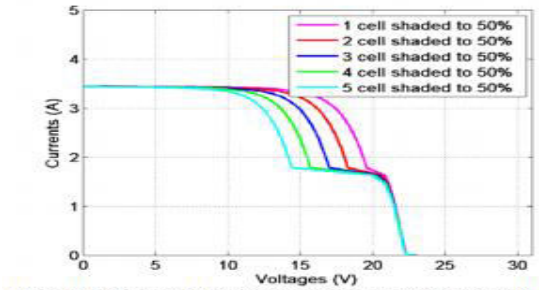

Fig 6.Effect of using bypass diodes across each solar cell

Bypass diodes will allow current to pass around shaded cells and thereby reduce the power losses through the module. When the module becomes shaded the bypass diode becomes forward biased and begins to conduct current through itself. All the current greater than the shaded cells new short circuit current is bypassed through the diode , thus reducing drastically the amount of local heating at the shaded area.

To demonstrate the effect of using bypass diodes across number of series connected cells, the characteristics of 18 cells among which one cell shaded across bypass diode is modelled and series connected to the normal 18 cells. The diode limits the reverse voltage to -0.7 volts and become forward biased as the current in the series connection changes because of shading. It bypasses the photo generated current more than that of shaded cell. The arrangement of bypass diode in solar module is shown in fig 9.

In case of mismatching this measure increases the power production of the PV arrays but introduces multiple local maximum in its power versus voltage characteristics as seen in fig.8, fig.10 and fig.11 which can confuse maximum power point tracking (MPPT) algorithm leading it to lower performances

3.2.3 Homogeneous Shading

When all the modules in the string do not receive same amount of irradiance, the effect can be termed as homogeneous shading. This phenomenon can occur when different modules connected in series has different tilt angle (for example building integrated PV applications) so that they can receive different irradiation. In this conditions bypass diodes may conduct as the modules in the string have different current. This can cause significant mismatch effect. Further, the power and efficiency of the string will be reduced. To continue further on this discussion 10 series connected modules were considered at operation in homogeneous shading conditions (fig 7). As an example, 6 modules are assumed to have 100% irradiance with MPP of 56.53 W each whereas remaining 4 modules receives only 75% irradiance because of different tilt angle. The MPP power of the shaded string is 460.9 W. Due to this situation shading loss is 18.47% including MPP mismatch loss of 8.95 %. The module based MPPT can harvest more energy than conventional string system because of individual MPP tracking.

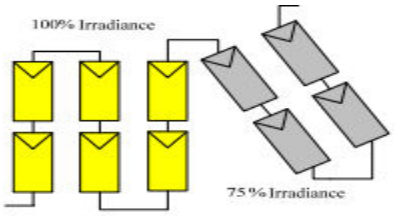

Fig. 7 Homogeneous Shading (different tilt angle)

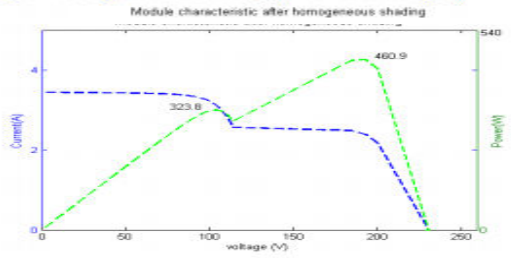

Fig 8: Effect of Homogeneous shading in string (fig.7) characteristics.

3.2.3 Partial Shading

Bypass diodes can reduce performance degrading when partial shading occurs. In order to demonstrate this string configuration as shown in fig. 9 is used. The single cell of a module is shaded to 25%. The MPP of this module is 45.61 W. This in turn is series connected to the normal modules having 56.53W MPP each. When the shaded module is series connected with other non shaded module, additional mismatch losses occurs. The shading effect results in degraded

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string output because the current of series connected string in module is affected by shaded cell .The interesting phenomenon in fig. 10 is when the 5 modules are connected in series and diode conduct to bypass the shaded cell string, the peak power becomes 252.5 W, which is higher than the value 243 W when all cell strings work together. It means it is more efficient to completely remove the compromised cell than to have it operate at partial capacity and degrade the performance of other cells in string [7]

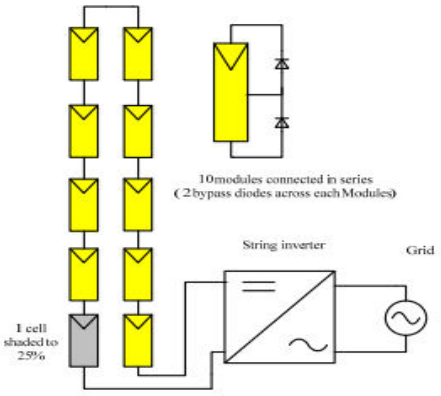

Fig. 9 Series connection of 10 modules

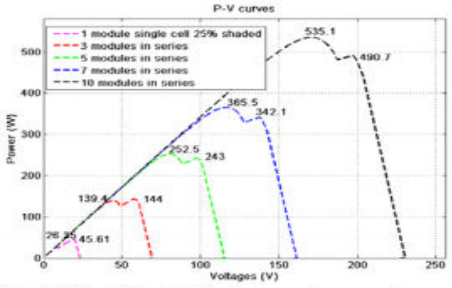

Fig. 10 Effect of partial shading in series connection

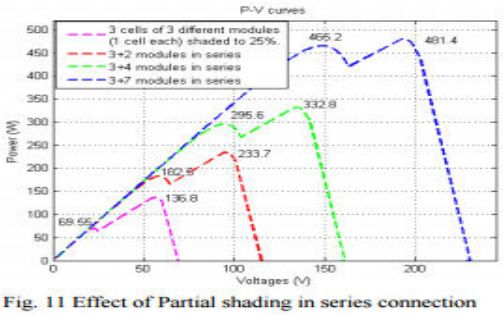

Fig. 11 Effect of Partial shading in series connection

4. CONTROL STRATEGY OF THE PROPOSED SCHEME

The control strategy of the proposed scheme is depicted in Fig. 5. The controller is designed to fulfill the following objectives: i) both sub arrays operate at their corresponding MPP simultaneously, ii) sensing of output voltages, vco1 and vco2 are not required, iii) ig is sinusoidal and is in-phase with vg throughout the operating range. Two separate MPP trackers and two proportional integral (PI) controllers are employed to determine the value of Ppv1 and Ppv2 which are required

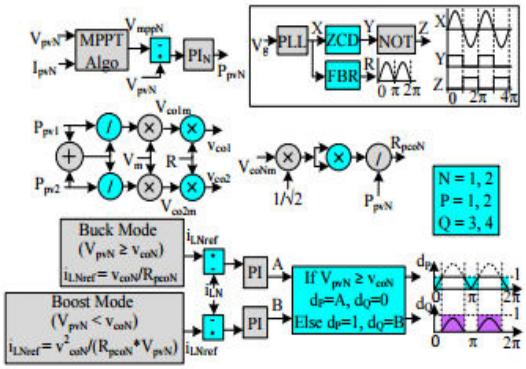

Fig. 5. Control configuration of the proposed inverter

to estimate Vco1m and Vco2m. Using (12), Vco1m and Vco2m are determined where the information of Vm is obtained from the phase locked loop (PLL). A rectified version of a unity sinusoidal function, R is generated from a unity sinusoidal function, X, synchronized with vg, and is obtained from the same PLL. R is multiplied with Vco1m and Vco2m to estimate vco1 and vco2. Hence, two voltage sensors which otherwise would have been required to determine vco1 and vco2 get eliminated. Vpv1 and vco1 are compared to decide about the mode of operation (buck mode or boost mode) of CONV1, while Vpv2 and vco2 are compared to determine the mode of operation of CONV2. RMS values of vco1 and vco2 are estimated which are then subsequently squared and are then divided by Ppv1 and Ppv2 to obtain the emulated effective resistances, Rpco1 and Rpco2 of the two component converters. Subsequently the reference current, iL1ref of L1 and the reference current, iL2ref of L2, are synthesized by utilizing in the buck mode ,

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$$i_{L1ref} = \frac{v_{co1}}{R_{pco1}} \quad \text{and} \quad i_{L2ref} = \frac{v_{co2}}{R_{pco2}}$$

while for boost mode is used to generate iL1ref and iL2ref.

$$i_{L1ref} = \frac{v_{co1}^2}{R_{pco1} V_{pv1}} \quad \text{and} \quad i_{L2ref} = \frac{v_{co2}^2}{R_{pco2} V_{pv2}}$$

The sensed inductor currents, iL1 and iL2 are compared with their corresponding references iL1ref and iL2ref . The errors so obtained are processed through two separate PI controllers to generate the required sinusoidal duty ratios for the switches, S1 and S2 during buck mode. Similarly, two separate PI controllers are engaged to process the generated errors to synthesize required sinusoidal duty ratios for switches S3 and S4 during boost mode. Signal Y is used to generate gating signals for S5, S8 while signal Z is used to generate gating signals for S6, S7 of the grid frequency unfolding inverter.

4. SIMULATION STUDY

To demonstrate the efficacy of the proposed inverter a PV array consisting of two PV sub arrays while each of the sub array having four series connected Canadian solar polycrystalline modules 'CS6P-165PE' [25] is considered. The MPP parameters of each sub array at standard test condition (STC) are as follows: Vpv1 = Vpv2 = 116 V, Ipv1 = Ipv2 = 5.7 A and Ppv1 = Ppv2 = 661 W.

The variation in isolation level and temperature with respect to time which is considered for the two sub arrays to demonstrate the effectiveness of the proposed inverter. Estimated variation of Ppv1, Ppv2 along with the other parameters Igm, Vco1m, Vco2m, peak of iL1 (IL1m) and peak of iL2 (IL2m) are also indicated. Fig. 6(a)-(c) represents the variation of Ppv1, Ppv2, Vpv1, Vpv2, Ipv1, Ipv2 of the two sub arrays and also demonstrate the ability of the proposed inverter to operate the two sub arrays simultaneously at their respective MPP. Variation in ig, iL1, iL2, vco1 and vco2 along with their magnified versions for two different isolation levels are depicted in Figs. 7 to 9.

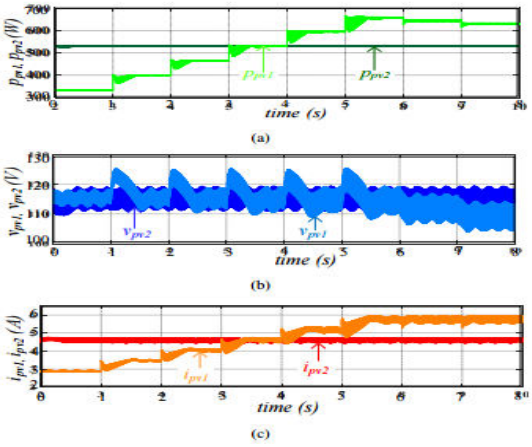

Fig. 6. Simulated waveform: Variation in (a) p_{pv1} and p_{pv2}, (b) v_{pv1} and v_{pv2}, (c) i_{pv1} and i_{pv2} during entire range of operation

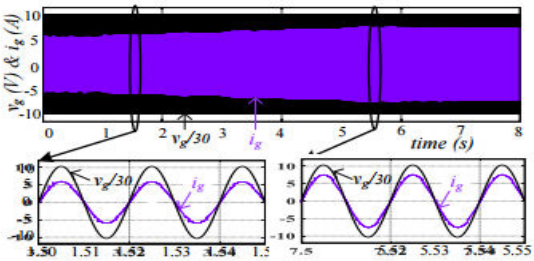

Fig. 7. Simulated waveform: v_g and i_g and their magnified views

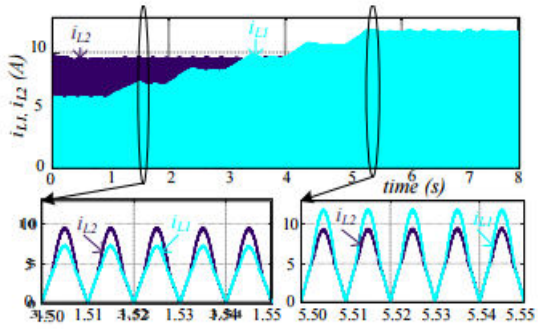

Fig. 8. Simulated waveform: i_{L1} and i_{L2} and their magnified views

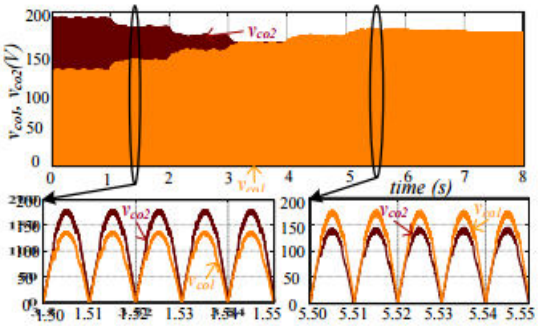

Fig. 9. Simulated waveform: v_{co1} and v_{co2} and their magnified views

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4.1 EXPERIMENTAL VERIFICATION

A 1.5 kW laboratory prototype of the proposed inverter is fabricated and detailed experimental studies have been carried out to demonstrate the effectiveness of the proposed scheme. In order to realize P V1 and P V2 two programmable EPS PSI9360-15 power supplies having solar PV emulation feature are utilized. The photograph of the experimental prototype is shown in Fig. 10.

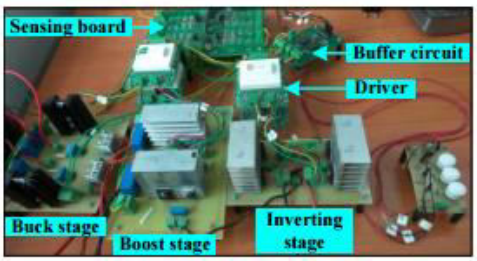

Fig. 10. Experimental prototype of the proposed inverter

5. CONCLUSION

A single phase grid connected transformer less buck and boost based PV inverter which can operate two sub arrays at their respective MPP was proposed in this paper. The attractive features of this inverter were i) effect of mismatched environmental conditions on the PV array could be dealt within an effective way, ii) operating efficiency achieved, ηeuro = 97.02% was high, iii) decoupled control of component converters was possible, iv) simple MPPT algorithm was employed to ensure MPP operation for the component converters, v) leakage current associated with the PV arrays was within the limit mentioned in VDE 0126-1-1. Mathematical analysis of the proposed inverter leading to the development of its small signal model was carried out. The criterion to select the values of the output filter components was presented. The scheme was validated by carrying out detailed simulation studies and subsequently the viability of the scheme was ascertained by carrying out thorough experimental studies on a 1.5 kW prototype of the inverter fabricated for the purpose.

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