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A LOW-POWER HIGH-SPEED CMOS COMPARATOR FOR PRECISE APPLICATIONS

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Abstract- In this paper, wepresent the high speed and low power design of a CMOS comparator for ADC applications. This CMOS dynamic comparator iscomposed of two stages, the decision stage and hold stage.The comparatoris operated in three different phases. First phase is reset, second phase is decision or evaluation and third phase is hold phase which stores the evaluation result for a specific time interval. In this proposed circuit the first stage power consumption is lessen by limiting the pre-amplifier's voltage swing to Vdd/2. At the evaluation phase, voltage swing constraint provides a vigorous drive which improves comparison speed. The power is dissipated when clk3 is low, and in reset and evaluation no power is dissipated. Overall power consumption is decreased and energy efficiency can be improved. The important point in the proposed comparator is the length of time that it is in low state. It is shown that in the proposed dynamic latched comparator have less dissipated power and time delay when compared with the NMOS and PMOS comparators. The Proposed design of this comparator is fabricated in a tanner EDA (Electron Design Automation) tool with 16.1 version of 18nm technology gives significant improvement in the power and delay

Index Terms—Dynamic Comparator, High Speed, Low-Offset Comparator,Low Power, Two-Stage Comparator.

I-INTRODUCTION

The fast growing electronics industry is pushing towards high speed low power analog to digital converters. Comparators are used in electronic devices which are mainly used in Analog to Digital converter (ADC). In ADC they are used for quantization process, and are mainly responsible for the delay produced and power consumed by an ADC. The Comparators are also used for data transmission applications, switching power regulators and many other applications. Designing high-speed comparators becomes more challenging when working with smaller supply voltages. In other words, for a given technology, to attain high speed,

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transistors with increased width and length values are required to compensate for the reduction of supply voltage, which also increased in chip area and power. So, the transistor width and length are adjusted accordingly for minimum power consumption and maximum operating speed. A model for the comparator is developed and discussed, and its functionality is verified by showing a comparison of result obtained for the proposed model and the existing model. The comparator is basically excluded from application to the high speed A/D converters with high resolution owning to its large offset voltage which significantly affects the resolution. As a consequence, the preamplifier based comparator topology in which an amplifier is added before a latched comparator, aiming at achieving small offset voltage and high speed, has been developed. The preamplifier based comparator, which combine of an amplifier and a latch comparator can obtain high speed and low power dissipation. Thus, by considering factors of speed and power dissipation, preamplifier latch comparator is the choice of A/D converters. The designed comparator consists of three stages namely input stage, decision stage and output stage. The input stage (pre amplification) amplifies the input signal to improve the comparator sensitivity and isolate the input of the Comparator from switching noise coming from positive feedback stage. The final stage is the output stage (post amplification) and the final component of the comparator design is the output buffer or post-amplifier.

This remaining paper is organized as follows. The section-II discuss the existing method, in section-III presents the proposed method and the section-IV and V are discuss about simulation results and conclusion.

II-EXITING METHOD

II-INMOS Two-StageDynamic Comparators

The two-stage version of the NMOS two-stage dynamic comparator [5], [6] is comprised of a preamplifier and a latch. At the first phase which is called reset phase, clk is set to “1” and clkbar is set to “0” to reset the first and second stages of the comparator to GND and VDD, respectively (avoiding hysteresis). When, clk changes to “0” and clkbar changes to “1” thenthe evaluation phase is begin. In this phase, the parasitic capacitors of the output nodes of the preamplifier begin to being charged differentially based on the input differential signal (Vin+ − Vin−). When the common voltage at the output of the preamplifier becomes higher than the threshold voltage of an NMOS transistor (M10,11 in Fig. 1), the latch is turned on and amplifies its input differential voltage until it provides a rail-to-rail differential signal. In fact, the latch employs a positive feedback circuit to provide a fast amplification. Simultaneously, the output voltages of the preamplifier are charged to VDD. As a result, considering the large sizing of M3 and M4 which causes large parasitic capacitors at O1+ and O1− nodes, a low-offset comparator demands high power consumption. In addition, a longer time is required to charge the output voltages of the preamplifier stage to a level higher than an NMOS threshold voltage. In fact, during the evaluation phase the latch stage is not activated until the output

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voltages of the first stage are large enough to turn on the input NMOS transistors of the latch. Unfortunately, this delay is uncontrollable and varies with the input Vcm of the comparator. Moreover, when the latch starts working the speed is low, since the overdrive voltage of M10,11 is almost zero and takes time to increase.In the NMOS two-stage dynamic comparator, after a delay from the beginning of the evaluation phase, a differential voltage appears at the inputs of the latch (at O1− and O1+ nodes.). This differential voltage must be large enough to eliminate the effect of the latch on the input referred offset voltage and strongly activate the latch stage. Let us name this delay as the optimum delay.

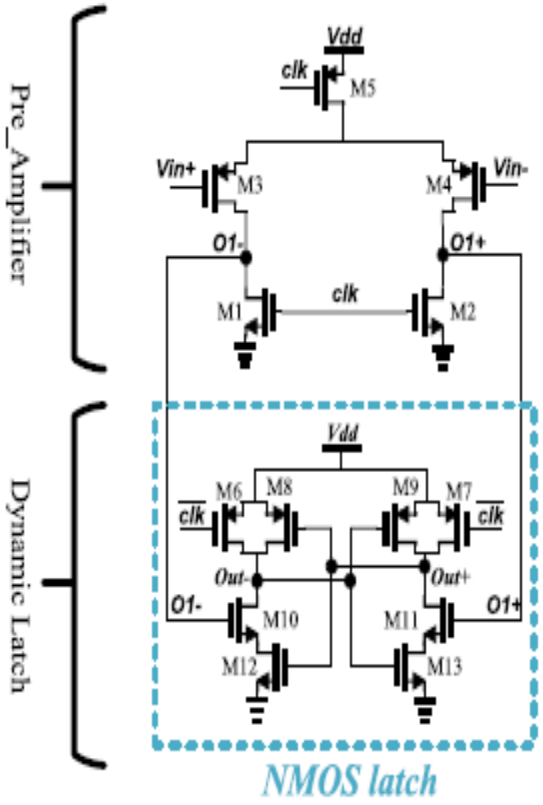

Figure 1(a): NMOS two-stage dynamic comparator.

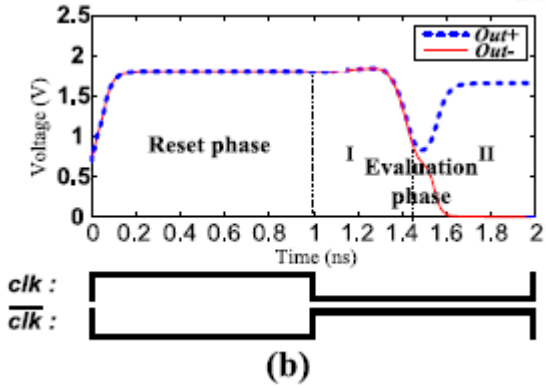

Figure 1(b):Output Waveform and Clock Signal.

The current of M5 is determined by the power consumption and speed criteria and the parasitic capacitors at O1+ and O1− are mostly the parasitic capacitors of M3,4 which are determined by the offset criterion. With an efficient design methodology, this problem may be alleviated; however, this fundamental problem still exists. The proposed comparator eliminates the problem inherently and efficiently makes it possible to have the optimum delay in the two-stage dynamic comparators. Therefore, it reduces the power consumption and improves the speed.

II-II PMOS Two-Stage Dynamic Comparator

The PMOS two-stage dynamic comparator is shown in Fig. 2(a). In contrast to the NMOS comparator, a PMOS latch (a latch with input PMOS transistors) is used in the latch which is activated with a predetermined delay during the evaluation phase [tamp, as shown in Fig. 2(b)]. This delay is supposed to be the optimum delay. At the reset phase, the clk, clkb1, and clkb2 hold logic “1” to discharge the output

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voltages of both preamplifier and latch to GND. At the evaluation phase, first the clk and clkb1 are toggled to logic "0" to start preamplification (charging the parasitic capacitors of O1+ and O1− nodes differentially). During this phase, the cross-coupled circuit increases the differential voltage (Vidl = [VO1+−VO1−]) slowly (since M4,5 are mostly in sub threshold region) and reduces the common mode voltage (Vcml = 0.5 × [VO1+ + VO1−]) to provide a strong drive for the input PMOS latch stage. Increasing Vidl (means larger preamplifier gain) further eliminates the effect of the latch on the input referred offset voltage.

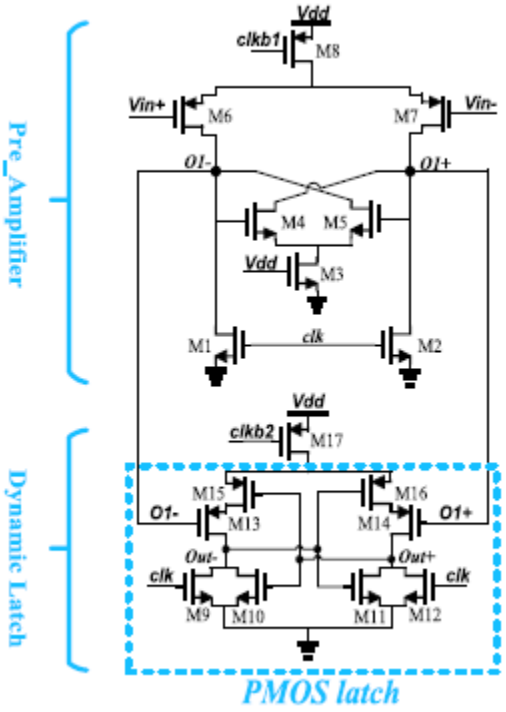

Figure 2(a): PMOS two-stage dynamic comparator.

Increasing Vidl (means larger preamplifier gain) further eliminates the effect of the latch on the input referred offset voltage. Also, larger Vidl results in a smaller latch delay. Decreasing Vcml enhances the speed of the comparator, since pMOS transistors are used at the input of the latch (M13,14). Finally, clkb2 is toggled to logic "0" to activate the latch. Simultaneously, clkb1 is changed to logic "1" to turn off the current source of the preamplifier in order to avoid excess power consumption. Amplification of Vid is kept going during this phase because the cross coupled circuit is still working independently of the current source (M8). Meanwhile, Vcml is kept reducing by M3−5.

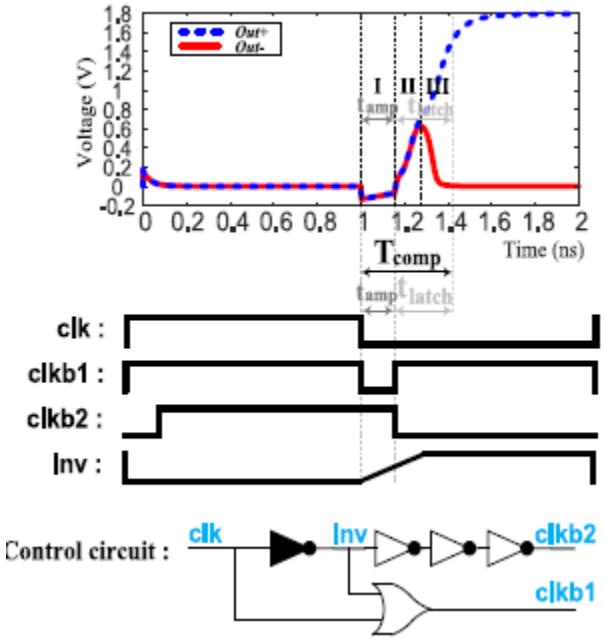

Figure 2(b): Output Waveform and Clock Signal.

The control signals are implemented using a local clock generator as shown in Fig. 2(b), which consumes a small amount of power. The black inverter is designed carefully to adjust the delay. Instructively, the PMOS two-stage dynamic comparator is robust

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against overlapped control signals, since overlapped signals only slightly affect the power consumption and have no effect on the precision. In the PMOS two-stage dynamic comparator circuit, the delay of the evaluation-phase is long enough to achieve the minimum required preamplification gain for a given speed and latch offset elimination. Thanks to the cross-coupled circuit (M3−5), during the first step of the evaluation phase, the differential voltage at O1+ and O1-nodes increases; however, the common-mode voltage of those nodes is kept low. Therefore, for a sufficient evaluation phase delay, tamp, Vcml (= 0.5 × [VO1+ + VO1−]) is pulled down to activate the pMOS latch strongly. Also, the larger Vidl boosts the latching process (speed). Consequently, the delay of the comparator will be small and almost flat over a wide range of the input Vcm. Transition of clkb1 to logic "1" limits the power consumption of the preamplifier which is the main part of the total power consumption. In the meanwhile, the cross-coupled circuit continues preamplification at no cost of power consumption. As another benefit, the delay time from beginning of the evaluation phase to beginning of the latching process is simply controllable and can be tuned at its optimum value. Without the cross-coupled circuit, the optimum delay could not be realized since a larger preamplification time reduces the VGS voltage of the following input PMOS transistors of the latch (worsening the speed and power). Therefore, the power, area, and offset contribution of the cross-coupled circuit is negligible. The cross-coupled circuit increases the differential voltage mainly when the preamplifier is turned off and enhances the speed; however, its main purpose is to reduce the input common-mode voltage of the latch.

III-PROPOSED METHOD

In today's world due to increase in demand for the portable battery powered devices, the necessity arises for dynamic latched comparators with high speed, low power consumption and full swing output. These comparators can become a part of high speed ADCs, sense amplifiers used in SRAM read/write circuitry and data receivers. The power consumption is of keen interest in achieving overall higher performance in ADCs. The main drawback of pre-amp based static comparators is its high power consumption. To minimize this problem CMOS dynamic comparators are often used that makes a comparison once in every clock period and requires much lesser power.

III-I Circuit Architecture

The proposed comparator architecture consists of two stages. The first stage is comprised of a preamplifier stage and the second stage is a latch stage. The first two stages are fed with clock Clk1 and Clk2. The mismatch effect inside the latch circuit is being overcome by separating the input transistors [1]. At the first phase both Clk1 and Clk2 are high which discharges the output node to the ground. During the second phase the Clk1 goes low which turns on the transistor M7 and M8 and the current starts to flow and charges up the node

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capacitor till Clk2 goes low. As soon as Clk2 goes low transistor M12 and M13 goes off which cuts the path from the input to the cross coupled latch.

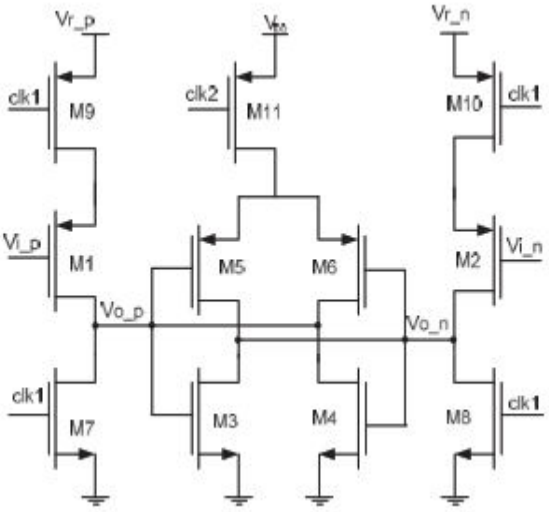

Figure 3: Differential dynamic comparator

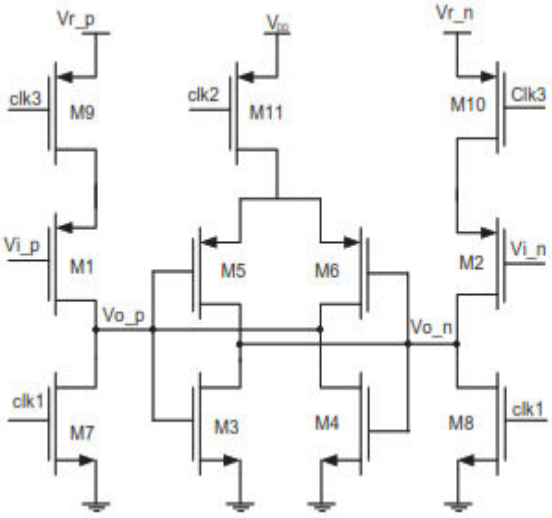

Figure 4: schematic of the Proposed Comparator

This separation helps to fight back the kickback noise which is generated at the latch during decision phase. The voltage difference between the input branches and the reference differential voltage gives rise to the current $I_{IN}+$ and $I_{IN}-$. This process takes place during the amplification phase. During the third phase the Differential voltage is boosted in the regenerative loop of the cross coupled inverter.

III-II Decision point

A comparator compares the input differential voltage with reference differential voltage V_{REF}diff. The output nodes Vout+ and Vout- are discharged to the ground at the beginning. The amplification starts as soon as the clock Clk1 goes low and Clk2 still remains high. The transistors M7 and M8 operate in linear region which acts as a resistor to the input transistor M5 and M6. At the beginning of the third phase the initial voltage at the output nodes are Vout+ = $I_{IN}+$ tamp/CL, Vout-=$I_{IN}-$tamp/CL. Once the comparator enters into the third phase the sign of the Vout+ and Vout- determines which way the comparator swings. The input currents are controlled by Vin+-$V_{REF}+$ and $V_{IN}-V_{REF}-$.

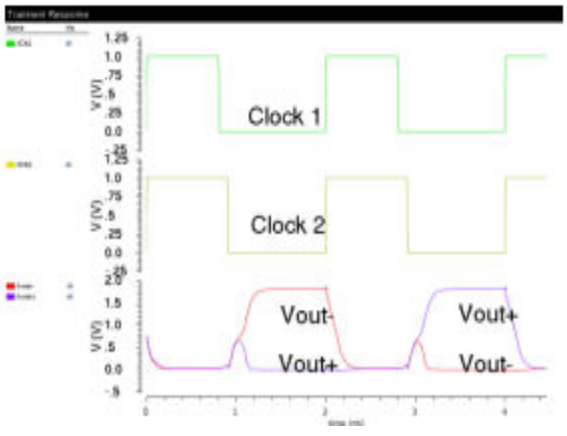

Figure 5: Output waveform showing the swing of the proposed comparator

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IV-SIMULATION RESULT S AND COMPARISON

IV-I Exiting Method Results

NMOS:

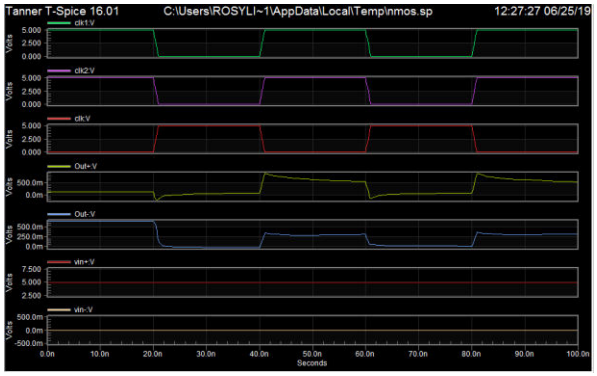

Figure 6: Typical NMOS output waveform and clock signal.

PMOS:

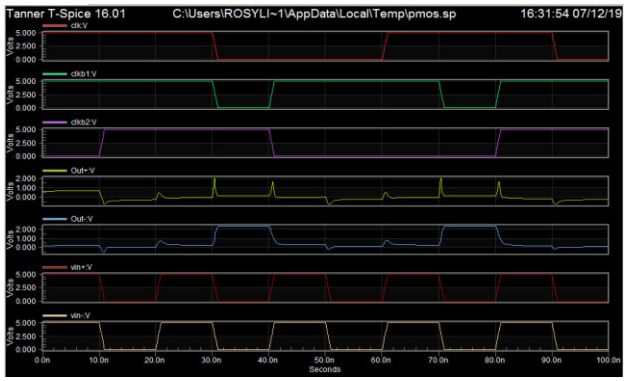

Figure 7: Typical PMOS output waveform and clock signal.

IV-II Proposed Results

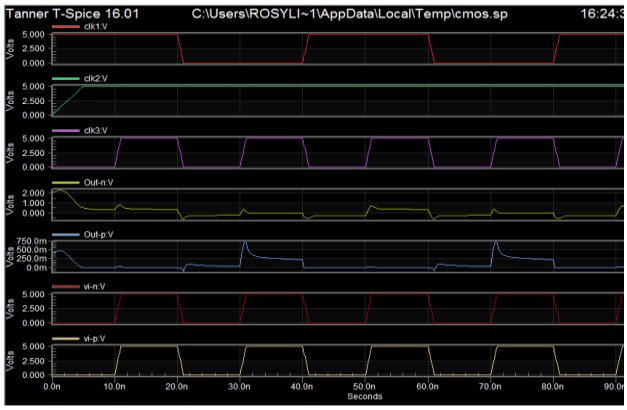

Figure 4.3:Output Waveform of Proposed CMOS Comparator.

The output waveforms of NMOS, PMOS and CMOS comparators are as shown in above figures.

These waveforms show the evaluation phase and reset phases of the comparators.

IV-III Comparison Table

Type of comparator	Area	Delay	Power
NMOS	28	1.73sec	1.1^{e-004}
PMOS	35	1.63sec	1.5^{e-004}
CMOS	26	0.83sec	2.0^{e-004}

V-CONCLUSION

A new CMOS dynamic comparator with low power, high speed and low offset voltage has been proposed by varying the area, delay and power. The proposed comparator was simulated in tanner EDA (Electron Design Automation) tool with 16.1 version of 18nm technology and their results are shown in the comparison table. The area and delay of the proposed comparator was reduced with cost of power consumption.

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