IMPLEMENTATION OF PV CELL FED ASYMMETRICAL MULTI LEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES

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**ABSTRACT-**

This paper proposes a new Asymmetrical multilevel inverter topology with reduced number of switches. This topology is superior to the existing multilevel inverter (MLI) configurations in terms of lower total harmonic distortion (THD) value and lower cost. The idea incorporates a new module setup comprising of four different voltage sources having voltage output levels in a specific ratio. Multilevel inverters have gained much attention for its operation involving applications ranging values of high power rating. This paper proposes a switching topology for asymmetric multilevel inverter utilizing less number of power electronics components. When the number of the output level increases, it requires more switching states and eventually the number of switching components. The increased number of switches results in higher switching losses which may lead to power loss, and reduction of efficiency of the overall conversion system. The salient feature of this proposed topology is that the module can be used as a sub multiple level structure and can be extended for any number of level with minimal increase in the switching components pho. The multilevel topology consists of several cells connected in series, each one connected to a string of PV modules. The adopted control scheme permits the independent control of each dc-link voltage, enabling, in this way, the tracking of the maximum power point for each string of PV panels. Additionally, low-ripple sinusoidal-current waveforms are generated with almost unity power factor. MLI is receiving tremendous popularity both in terms of topology and control scheme due to its good power quality, less total harmonic distortion (THD), reduced voltage stress across the switches, good electromagnetic compatibility, less switching losses. In extension A single-phase topology is extended for three-phase with PV input.

**I INTRODUCTION**

Multilevel inverter (MLI) was first introduced in 1975, since its invention the demand is growing rapidly in the field of DC/AC power conversion and associated applications [1]. MLI is key technology and plays crucial role in AC motor drives, uninterruptible power supplies, high-voltage DC power transmission, flexible AC transmission systems, static var compensators, active filters, electric and hybrid electric vehicles and integration and utilization of renewable energy sources [2]. In the field of

high-power medium-voltage DC/AC conversion, MLI is receiving tremendous popularity both in terms of topology and control scheme due to its good power quality, less total harmonic distortion (THD), reduced voltage stress across the switches, good electromagnetic compatibility, less switching losses and dv/dt stress. However, MLI possesses some drawback, that is, to increase output levels, the number of semiconductor switch requirement along with peripherals devices such as gate driver circuit, protection circuit and heat sink increases. Increased device count makes overall system complex, bulky and costly and reduces the reliability and efficiency of the converter. Traditionally, MLIs

are classified as; cascaded H-bridge (CHB), flying capacitor (FC) and neutral point clamped (NPC). In the past few decades, most of the literatures published shows the study on CHB, FC and NPC topologies with respect to their respective advantages and disadvantages [15] and these topologies are now widely referred to as the ‘classical topologies’. None of the classical topologies seem to be absolutely advantageous as multilevel solutions are heavily influenced by application and component count, cost and complexity considerations. Among the classical MLI, CHB has received wide attention due to its modularity and simplicity; however, the requirement of isolated source is a limitation of the topology [16]. A CHB MLI is composed of several H-bridge cell and isolated DC source. On the basis of voltage magnitude DC source, CHB is classified as symmetric and asymmetric configurations. In symmetric configuration, the magnitude of DC source is equal (*V1 = V2 = V3…*), whereas in asymmetric configuration magnitudes of DC sources are not equal (*V1 ≠ V2 ≠ V3….*). The asymmetric configuration of CHB produces higher number of voltage level as compared with symmetric configuration for same number of power switches [15]. Along with the exploration of CHB, researchers paid dedicated effort and attention to evolve newer application oriented topologies with reduced number of device count and complexity.

Consequently, in past few years, large numbers of topologies and control scheme have been proposed with reduced device count which utilizes a combination of unidirectional and bidirectional switches of different ratings, some of them are reviewed here briefly. In, symmetrical topologies of MLIs are discussed, the cost of these inverters is less due to low variety of DC sources, but the modularity of these MLIs is major concern in various applications. Similarly in, asymmetrical topologies of MLI with reduced number of switches are presented, but the requirement of large number of bidirectional switches is a major issue in these topologies. Topology of MLI presented in [22] utilizes low-frequency high-power switches due to which there is presence of lower-order harmonics in output waveform which is the major drawback. In topology incorporates multi-winding transformer due to which cost and complexity of the overall topology increases. A 4-level inverter topology is presented in, but the presented topology is unable to provide zero-voltage level which results in high root mean square value and harmonic energy is concentrated at switching frequency. In [28], another topology is presented for 5-level by utilizing four DC sources, whereas in conventional topologies up to 9-level can be reached by utilizing four DC sources. The topology presented in also reduces the number of controlled switches to a great extent for both symmetrical and asymmetrical MLIs, but the requirement of large number of isolated DC sources is the major drawback of these topologies. Existing literature reflects that most of the published MLI topologies in recent years are claiming higher outputs levels with reduced number of switches. However, great compromise has been made in terms of modularity, simplicity, number of bidirectional switches, variety of DC sources, voltage stress across switches, reliability and losses.

This paper focuses on symmetrical and asymmetrical MLI topologies and tries to solve the problems related to it. Two new topologies of symmetrical and asymmetrical MLIs are proposed using hexagon switch cell (HSC). The proposed topology is capable of producing 7/9/11 output levels by utilising seven controlled switches. Reduction of devices is based on reduction in number of insulated gate bipolar transistors (IGBTs), driver circuits, diodes, bidirectional switches, DC sources and heat sinks. The symmetrical and asymmetrical configurations of proposed topologies generate higher number of output levels with less number of switches comparatively. Qualitative improvement is based on reduction in blocking voltages on switches, variety of switches, variety of heat sinks, equal utilization of DC sources and improvement in fault tolerance capability of inverter. An exhaustive comparison of proposed topologies with classical topologies and most recent work in the field is carried out to highlight the novelty and benefit of the proposed topology.

**II PROPOSED MLI TOPOLOGIES**

**1 Proposed topology-1**

The configuration of Topology-1 is illustrated in Fig.1a. It consists of two DC voltage sourcesVS1 and VS2, along with capacitors C1 and C2 which forms voltage divider circuit. An auxiliary switch is formed by controlled switch S7 and four diodes D7, D8, D9 and D10 which is connected to HSC composed by six switches S1, S2, S3, S4, S5 and S6. When the values of the DC voltage sources are equal, that is, VS1 = VS2 then it can be referred as symmetrical MLI otherwise asymmetrical. Topology-1 is capable of producing 7-/9-/11-level output with certain combination of DC voltage source while incorporating only seven controlled switches. The output voltage level with particular combination of DC voltage source is summarized in Table 1. The generalized form of the proposed Topology-1 is shown in Fig.1b.

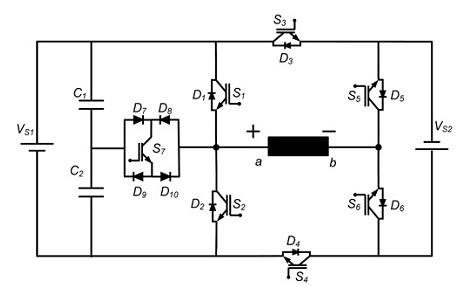


Fig.1 (a) Configuration of proposed Topology-1 for 9-level inverter

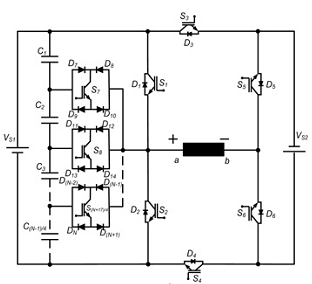
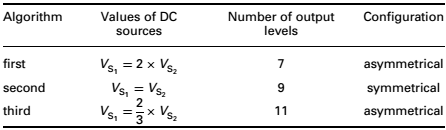


Fig.1 (b) Generalised configuration of proposed Topology-1

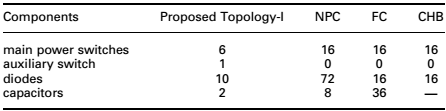
Fig.1 Proposed Topology-1

Table 1 Different combinations of DC voltage source for higher output voltage levels



To evaluate total number of component count, the Topology-1 is compared with classical topologies for 9-level output and summarized in Table 2.

Table 2 Comparison of different 9-level inverter topologies for symmetrical MLI



Main power switches: The proposed Topology-I in symmetrical configuration achieves 56.25% (seven instead of 16) reduction in the number of main power switches required as compared with classical topologies.

Power diodes: The proposed Topology-I in symmetrical configuration achieves 37.5% (10 instead of 16) reduction in the number of diodes required as compared with FC and CHB, whereas percentage of reduction increases to 86.11% (10 instead of 72) as compared with NPC. Similarly, it achieves 74% (2 instead of 8) reduction in number of capacitors required when compared with the NPC and 94.44% (2 instead of 36) reduction when compared with the FC.

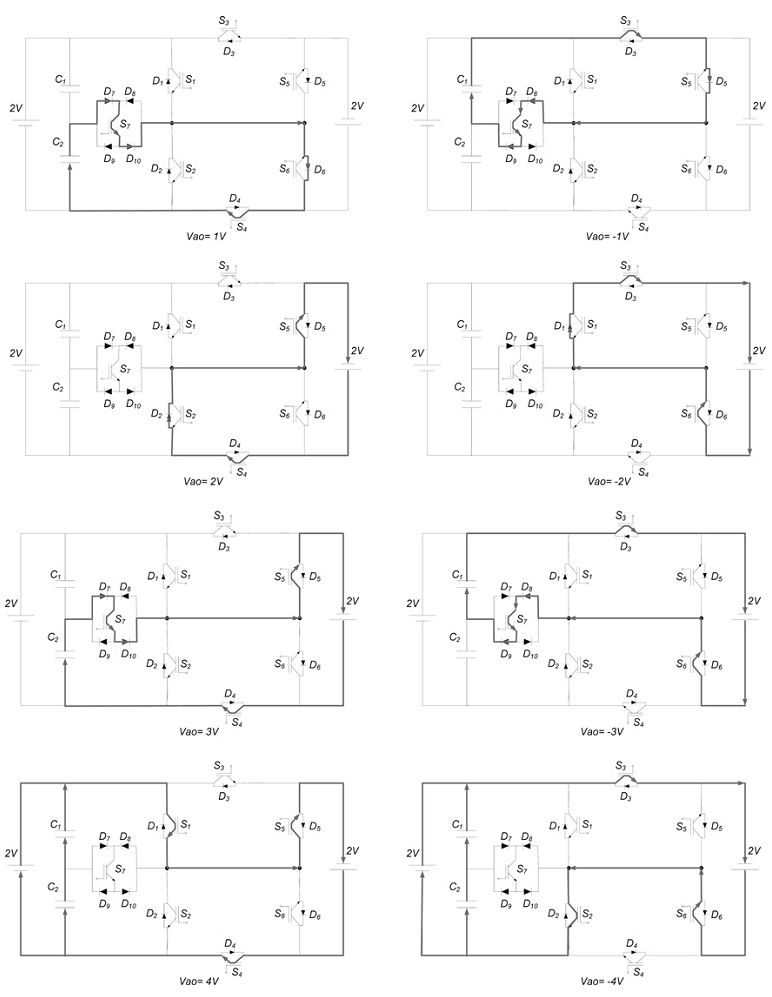


Fig.2 Different operating modes of Topology-I for 9-level output

The different operating modes and switching states along with corresponding output voltage levels for 9-level inverter are summarized in Fig.2 and Table 3, respectively. Similarly, the different switching states of Topology-1 in asymmetrical configuration for synthesizing 7-level and 11-level are summarized in Tables 4 and 5, respectively. The generalization of Topology-1 in symmetrical configuration for N-level output is given as

Total number of controlled switches required = (*N* + 19)/4 (1)

Total number of diodes required = (*N* + 1) (2)

Total number of DC sources required = 2 (3)

Total number of controlled switches required = (*N* - 1)/4 (4)

Table 3 Different switching states of Topology-1 for 9-level output

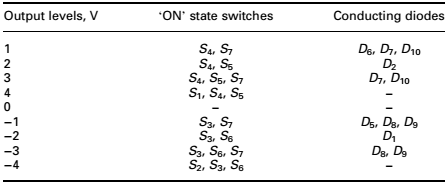


Table 4 Different switching states of Topology-1 for 7-level output (VS1 = 2V, VS2 = 1V)

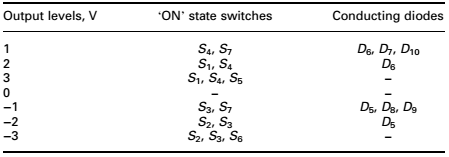
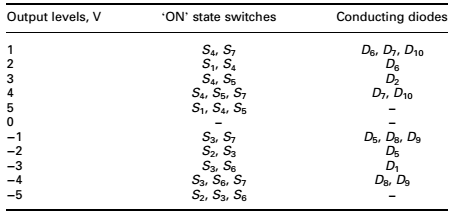


Table 5 Different switching states of Topology-1 for 11-level output (VS1 = 2V, VS2 = 3V)



**II PROPOSED TOPOLOGY-2**

The configuration of the proposed Topology-2 is shown in Fig.3a. It is modification of Topology-1 in the light of generalization for symmetric and asymmetric configurations. Topology-2 is composed of two auxiliary switches connected to HSC from both the sides. The composed switch network is supplied by two DC voltage source along with four capacitors. The generalized structure of Topology-2 is illustrated in Fig.3b. It contains series connection of several fundamental cells that can be operated for both symmetrical and asymmetrical configurations. Each cell contains eight controlled switches, 14 power diodes, two DC sources and four capacitors. The DC source on the left-hand side of HSC is numbered as *VL1*, *VL2*, *VLn* and on the right-hand side of HSC is numbered as *VR1*, *VR2*, ..., *VRn* (‘where n denotes number of series cell’). For symmetrical mode, the values of DC sources are equal and for asymmetrical mode the values of each DC sources are assigned according to the three different algorithms given. In conventional asymmetrical CHB MLI values of DC sources are increased in either binary combination (2:1) or ternary combination (3:1). In recently published work of asymmetrical configuration of MLI expanded the voltage ratio as 4:1 in [30], 5:1 in and 7:1 in [31]. The increase in ratio of DC voltage source above the ternary combination opens the possibility of

achieving higher number of output level with reduced number of switches in asymmetrical configuration. The different combinations of DC voltage source and corresponding output levels are summarized. Therefore, in the Topology-2 a new algorithm of DC source combination (fourth algorithm in Table6) is opted to achieve the higher number of output levels

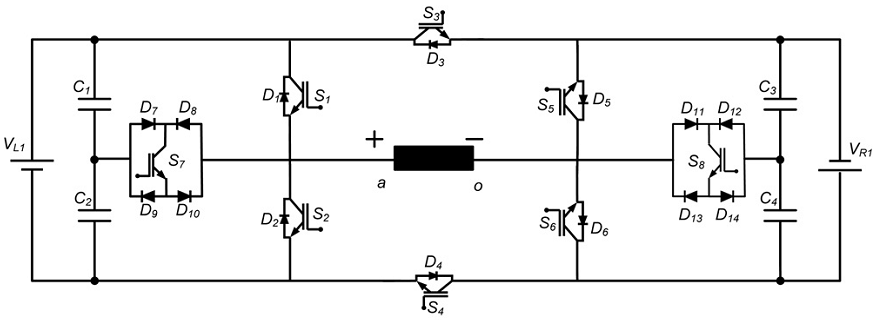


Fig.3 (a) Configuration of proposed Topology-2

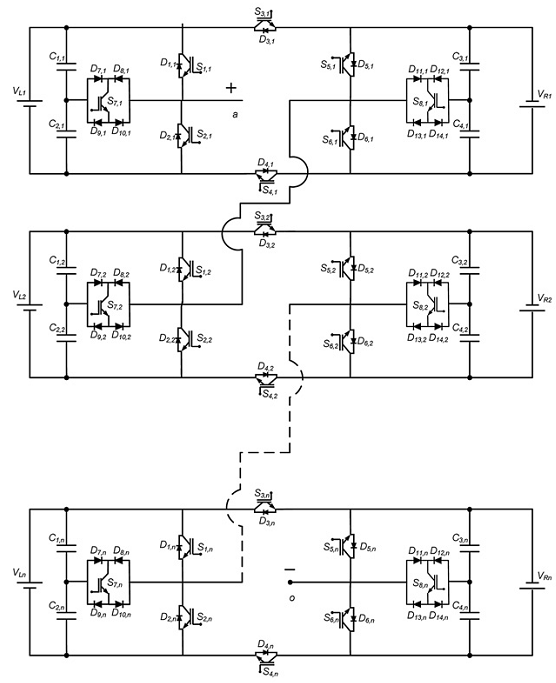


Fig.3 (b) Generalized structure of proposed Topology-2

Fig.3 Proposed Topology-2

Total number of DC sources = 2 × n (5)

Total number of capacitors = 4 × n (6)

Total number of controlled switches = 8 × n (7)

Total number of diodes = 14 × n (8)

**IV MULTILEVEL INVERTER WITH**

**REDUCED NUMBER OF SWITCHES**

In recent day’s Multilevel inverter (MLI) technologies become a incredibly main choice in the area of high power medium voltage energy control. Though multilevel inverter has a number of advantages it has drawbacks in the vein of higher levels because of using more number of semiconductor switches. This may leads to vast size and price of the inverter is very high. So in order to overcome this problem the new multilevel inverter is proposed with reduced number of switches. The proposed method is well suited for a high power application and it built with three Dc sources and six Switches. Multi carrier pwm technique is used for sine wave generation. The results are validated through the harmonic spectrum of the FFT window The result of the proposed MLI is compared with the conventional MLI and other seven level existing topologies In recent days MLI has drawn large interest in high power industry. They present a latest set of aspects to facilitate and utilized in reactive power compensation [3]. The unique arrangement of multilevel voltage source inverters allow them to achieve high voltages with the low harmonics not including the utilization of transformers or series connected synchronized switching devices The Diode clamped, Flying capacitor, Cascaded H-bridge inverter are the three main different multilevel inverter structures which are used in industrial applications with separate

dc sources. In flying capacitor and diode-clamped inverter there is a problem of capacitor

voltage balancing and this problem is overcome in cascaded H-bridge inverter. Conventional cascaded seven level multilevel inverter require twelve switches and three dc sources separately [8]. The main drawback in Conventional cascaded is that when levels are increasing it requires more number of semiconductor switches. As a result some alternations are to be made inorder to reduce the size and switch of the inverter. The next topology is made with three sources and nine switches and it yields the stair case waveform with the reduced total harmonic distortion compared to conventional multilevel inverter. Then the next topology is further reduced for two switches then it consists of three dc sources and seven switches where the harmonics are reduced. Again the seven level inverter is reduced with one switch but it also leads to increase in one of the dc sources so the topology is made of four dc sources and six switches [6]. But increase in one dc source is considers as one of the drawback of this circuit. By analyzing the advantages and drawbacks of the existing topologies. The new topology is proposed and discussed in this paper which overcomes the drawbacks of the existing topologies. The proposed topology is designed with three dc sources and six switches and also it consists of some additional features like minimum number of switches conducting at a specific interval of time, Further the multicarrier pwm method [5]. This structure is designed with six switches without H-bridge and four dc sources is used. Switches S6. S7 are used for generating the pulses in positive and negative sequences and the switch S1 is connected to the load it is used only when all the switches are open to produce zero voltage level. Switch S2, S3, S4 are used to generate the levels Vdc, 2Vdc and 3Vdc in both the positive and the negative levels. The circuit arrangement is shown in Figure 3. The switching topology of seven level six switches

**V.MATLAB/SIMULATION RESULTS**

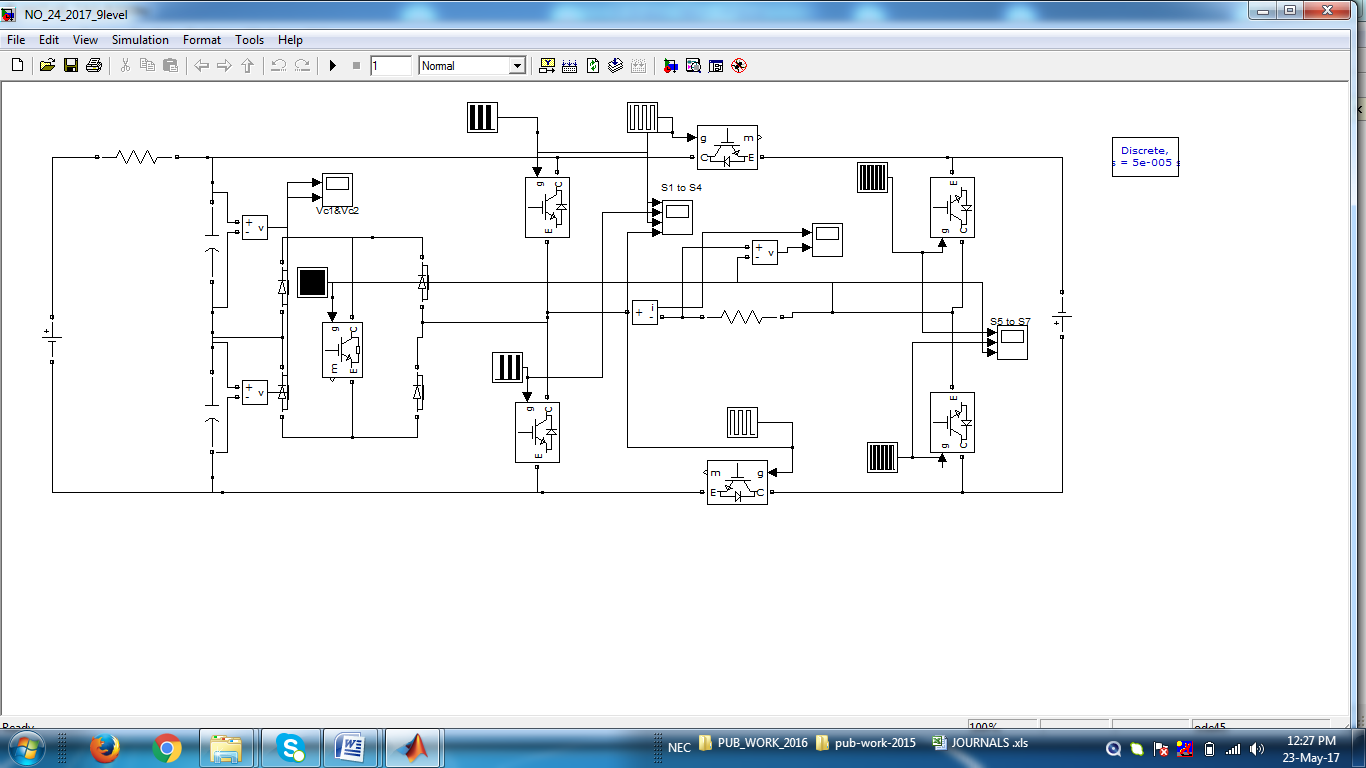


Fig 4 Matlab/simulation circuit of Nine Level Inverter

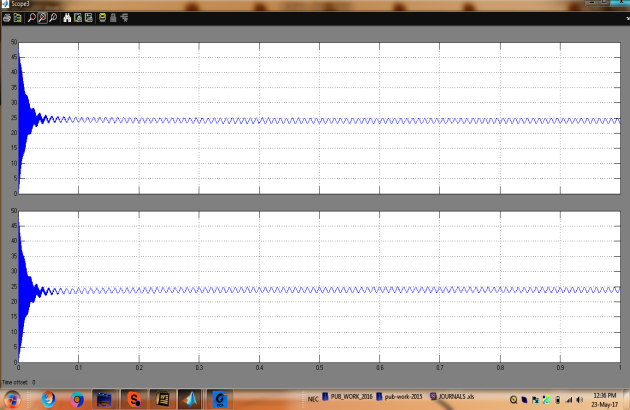


Fig 5 simulation wave form of source capacitor voltage

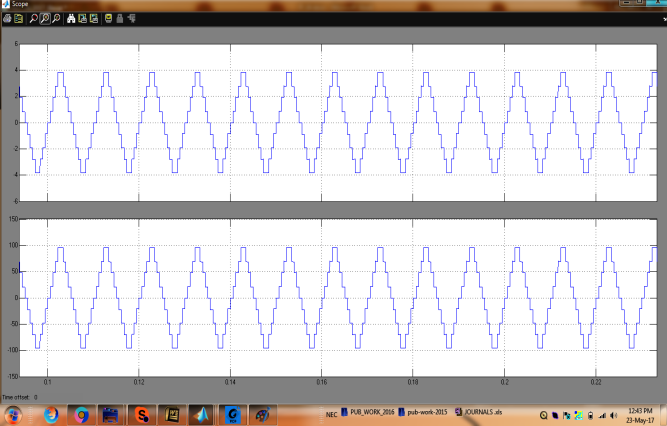


Fig 6 simulation wave form of output nine level voltages and current

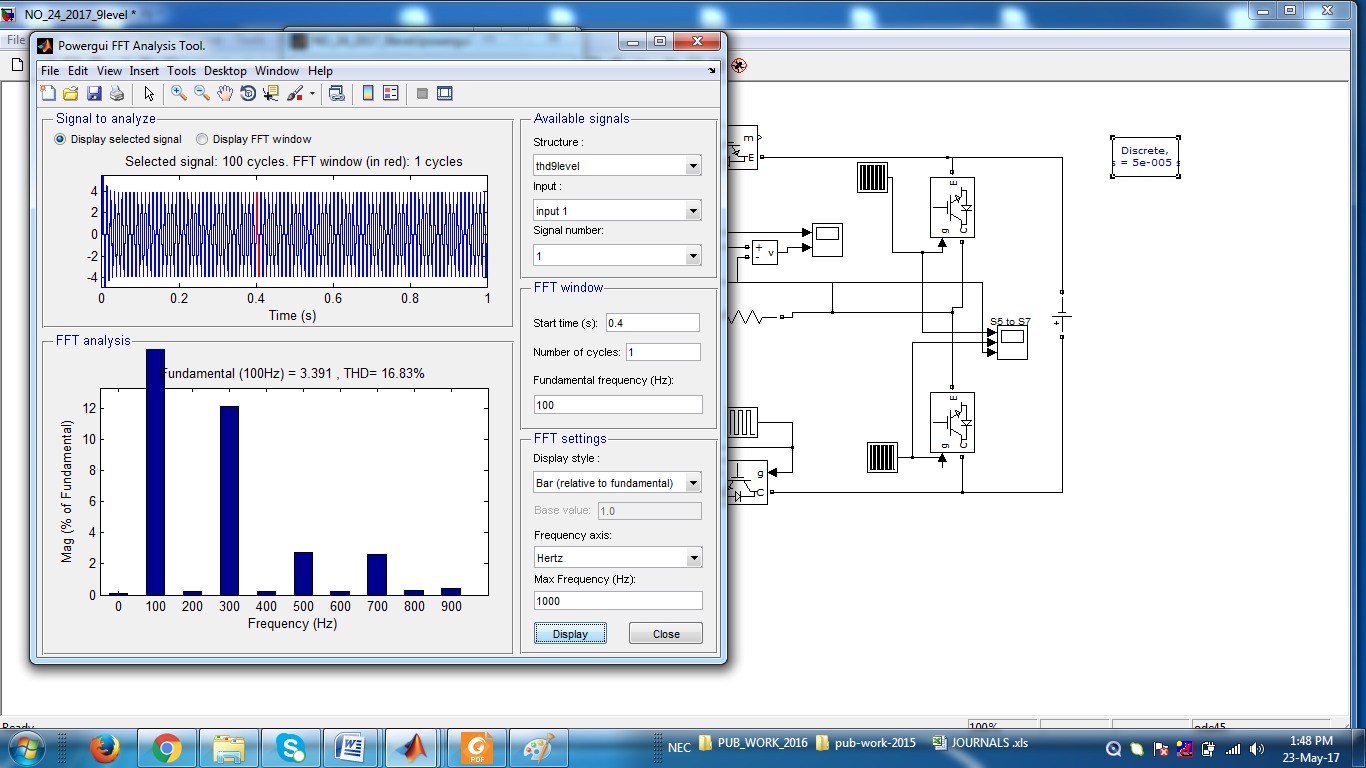


Fig 7 FFT analysis of 9-level THD

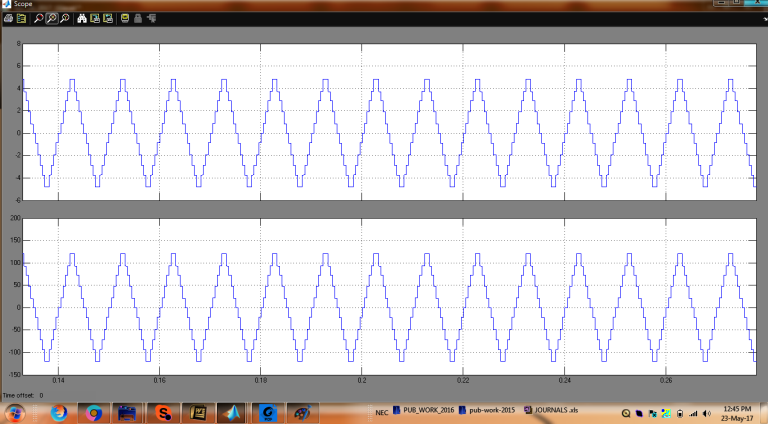


Fig 8 simulation wave form of output 11- level voltages and current

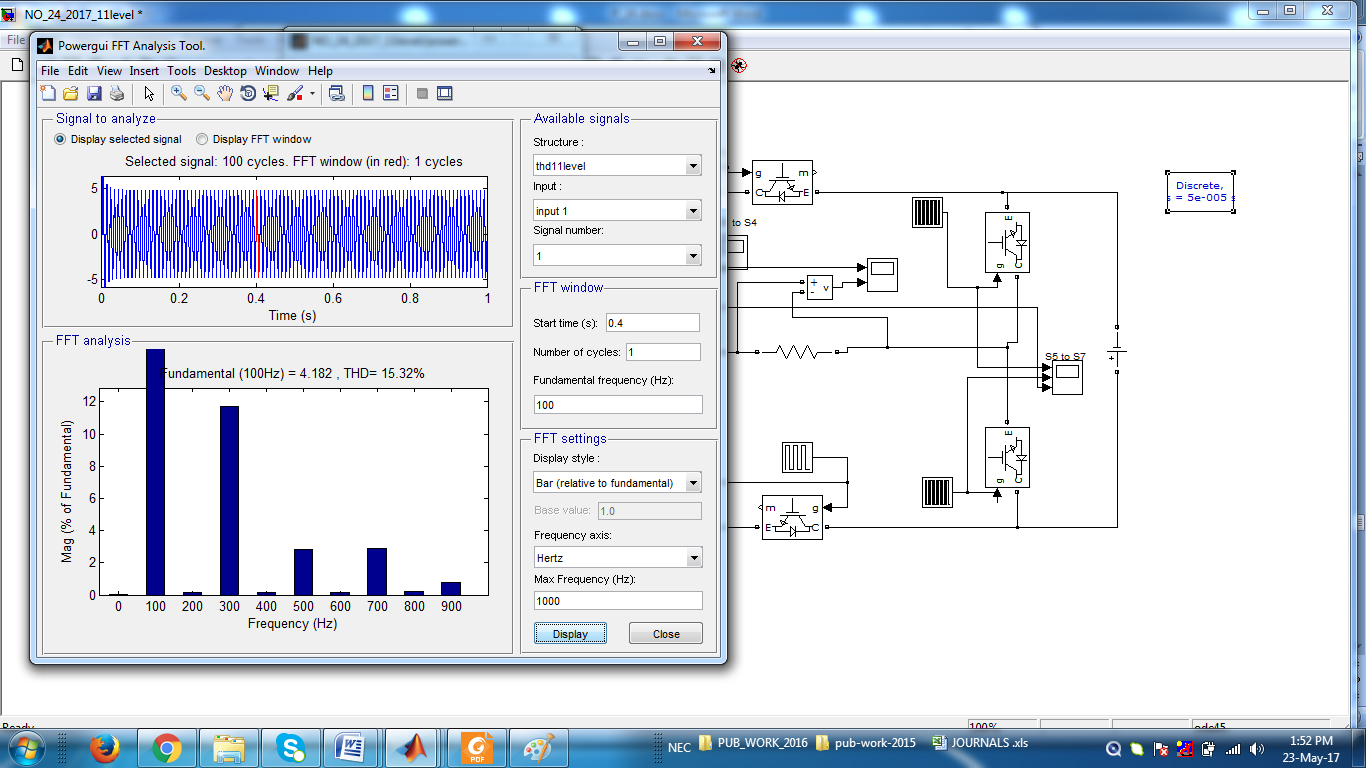


Fig 9 FFT analysis of 11-level THD

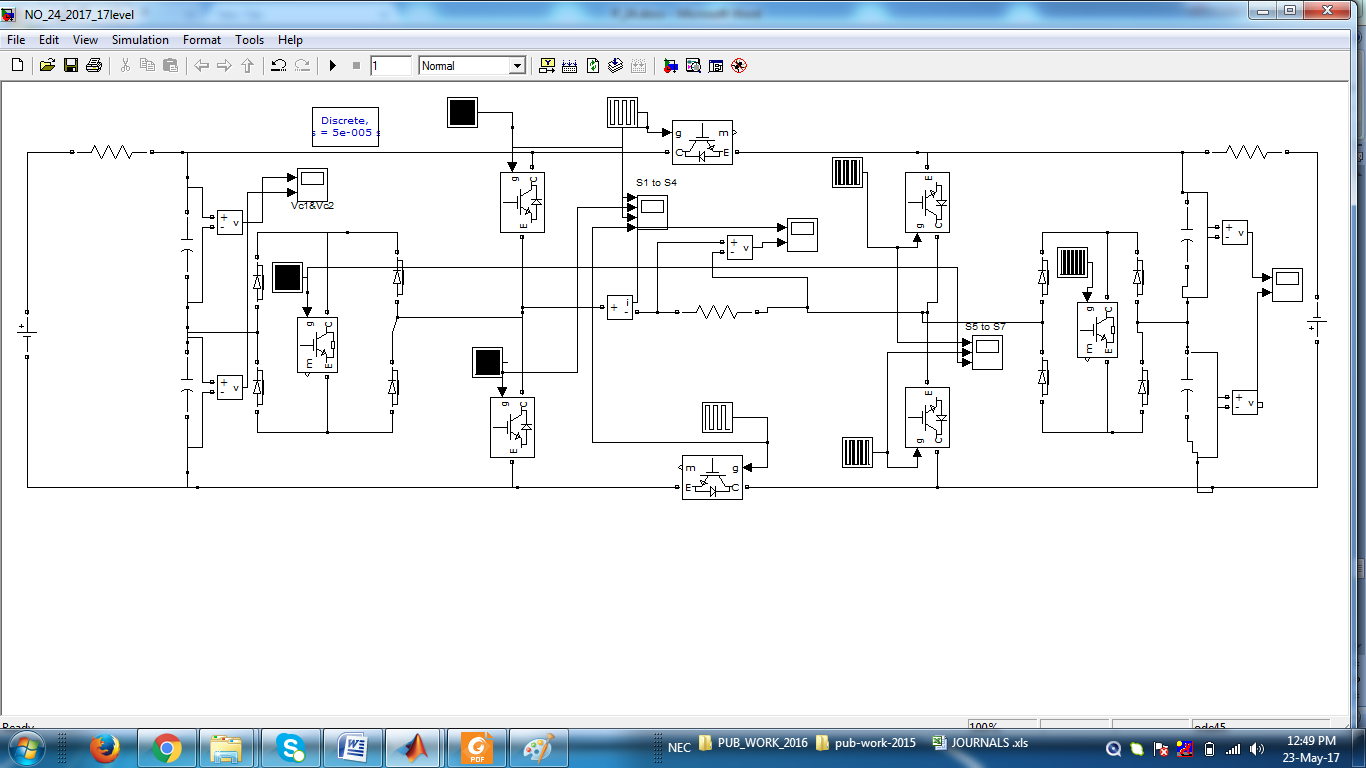


Fig 10 Matlab/simulation circuit of 17- Level Inverter

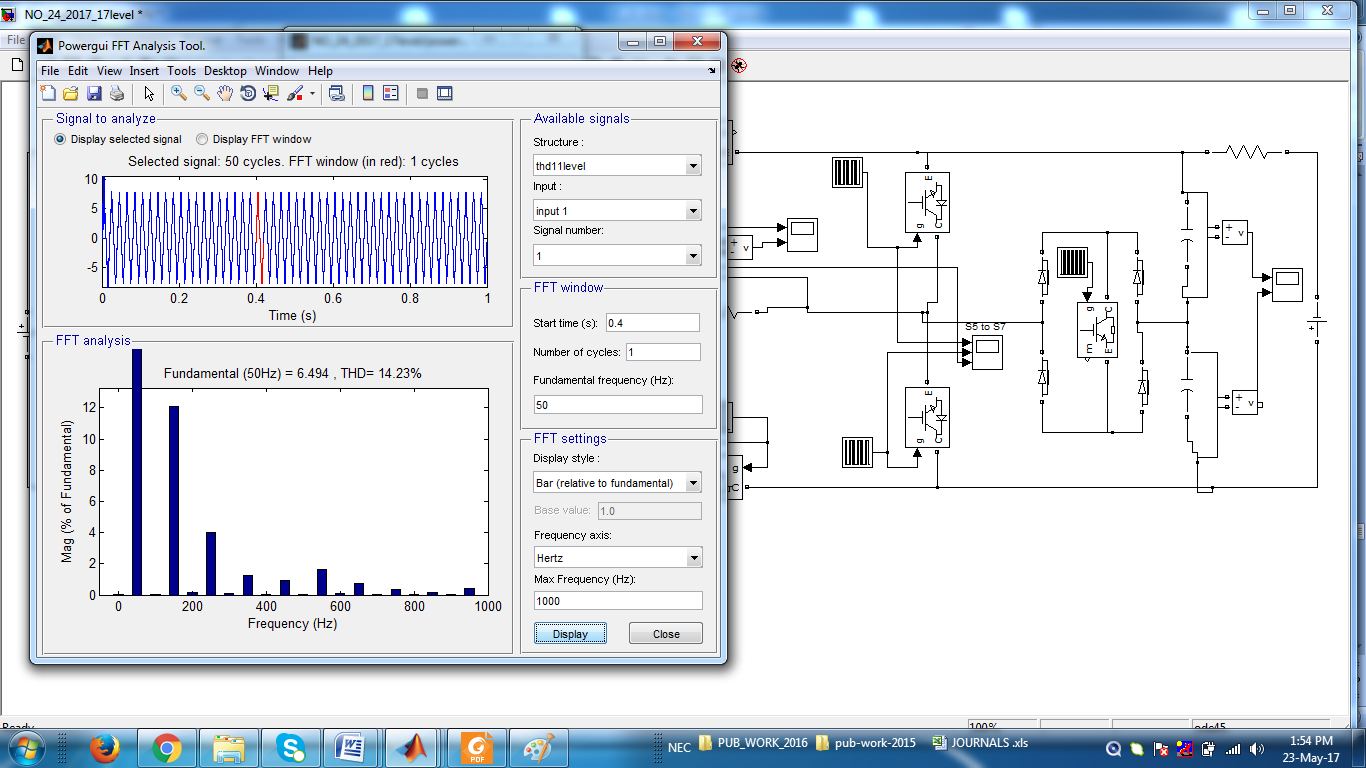


Fig 11 FFT analysis of 17-level THD

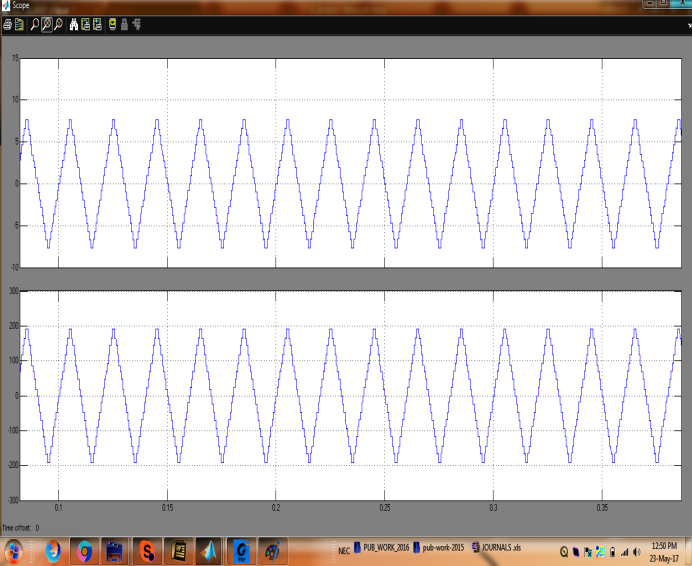


Fig 12 simulation wave form of output 17- level voltages and current

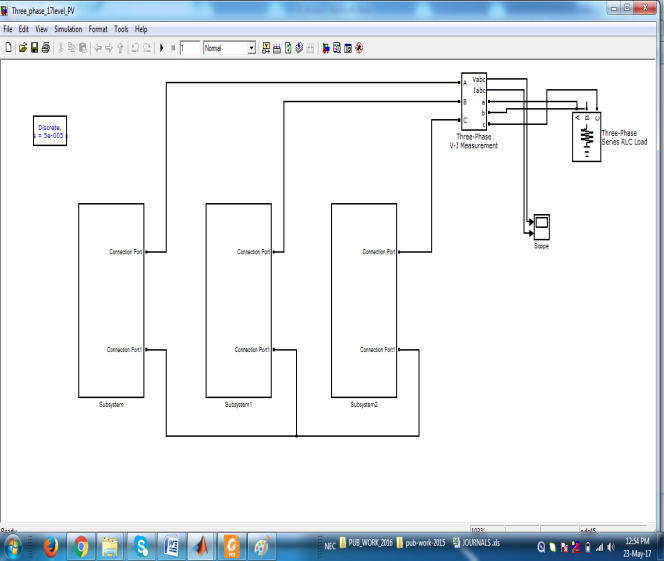


Fig 13 Matlab/simulation circuit of proposed three phase 17- Level Inverter

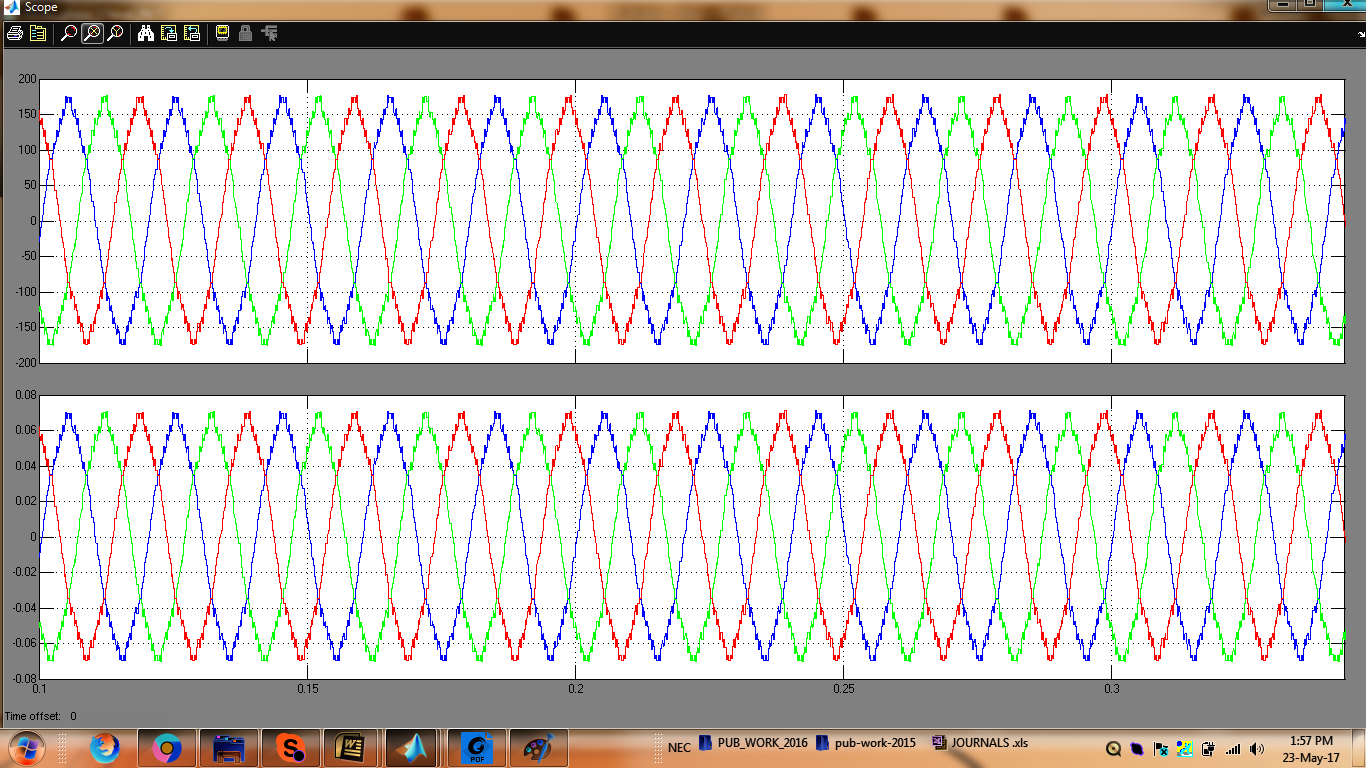


Fig 14 simulation wave form of output three phase 17- level voltages and current

**CONCLUSION**

In this paper, two novel topologies of symmetrical and asymmetrical configurations of MLI are proposed. For wide range of application (i.e. medium-to-high voltage), Topology-1 has been modified to cascaded version of Topology-1. To get maximum levels at output, again Topology-1 has been modified to Topology-1 and its operation is explained. First, the topology in symmetrical configuration is presented and a comparison is drawn for 9-level inverters. Then asymmetrical version of the proposed Topology-1 is given along with its operating states. The proposed topologies reduce the number of controlled switches, diodes, DC voltage sources and capacitor significantly when compared with conventional ones and other topologies presented recently. A wide range of comparison is made between the proposed topology and some of the recent published topology. The comparison shows that the minimum number of IGBTs, diodes, capacitors and blocking voltage of switches to maximum number of levels for output voltage is obtained. Finally, the proposed topologies have been verified through simulation and electrical feasibility has been tested experimentally.

**REFERENCES**

1 Baker, R.H., Bannister, L.H.:‘Electric power converter’. U.S. Patent 3 867 643, February 1975

2 Surendra Babu, N.N.V., Fernandes, B.G.: ‘Cascaded two-level inverter-based multilevel static VAr compensator using 12-sided polygonal voltage space vector modulation’, IET Power Electron., 2012, 5, (8), pp. 1500–1509

3 Patel, P.J., Patel, V., Tekwani, P.N.:‘Pulse-based dead-time compensation method for selfbalancing space vector pulse width-modulated scheme used in a three-level inverter-fed induction motor drive’,IET Power Electron., 2011,4, (6), pp. 624–631

4 Rabinovici, R., Baimel, D., Tomasik, J.,et al.: ‘Thirteen-level cascaded H-bridge inverter operated by generic phase shifted pulse-width modulation’, IET Power Electron., 2013, 6, (8), pp. 1516–1529

5 Rosas-Caro, J.C., Ramirez, J.M., Peng, F.Z.,et al.: ‘ADC–DC multilevel boost converter’, IET Power Electron., 2010, 3, (1), pp. 129–137

6 Fei, W., Wu, B., Huang, Y.:‘Half-wave symmetry selective harmonic elimination method for multilevel voltage source inverters’, IET Power Electron., 2011, 4, (3), pp. 342–351

7 Mathew, K., Mathew, J., Azeez, N.A.,et al.:‘Multilevel dodecagonal space-vector generation for induction motor drives by cascading three-level and two-level inverters’, IET Power Electron., 2012, 5, (8), pp. 1324–1332

8 Ma, K., Blaabjerg, F.:‘Thermal optimised modulation methods of three-level neutral-point-clamped inverter for 10 MW wind turbines under low-voltage ride through’, IET Power Electron., 2012, 5, (6), pp. 920–927

9 Suresh, Y., Panda, A.K.:‘Research on a cascaded multilevel inverter by employing three-phase transformers’, IET Power Electron., 2012, 5, (5), pp. 561–570

10 De, S., Banerjee, D., Siva Kumar, K.,et al.: ‘Multilevel inverters for low-power application’, IET Power Electron., 2011, 4, (4), pp. 384–392

11 Gupta, K.K., Jain, S.:‘Comprehensive review of a recently proposed multilevel inverter’, IET Power Electron., 2014, 7, (3), pp. 467–479.

12 Gupta, K.K., Jain, S.: ‘Topology for multilevel inverters to attain maximum number of levels from given DC sources’, IET Power Electron., 2012, 5, (4), pp. 435–446

13 Gupta, K.K., Jain, S.:‘Multilevel inverter topology based on series connected switched

sources’, IET Power Electron., 2013, 6, (1), pp. 164–174

14 Suroso, Noguchi, T.:‘Common-emitter topology of multilevel current-source pulse width modulation inverter with chopper-based dc current sources’, IET Power Electron., 2011, 4, (7), pp. 759–766

15 Nami, A., Zare, F., Ghosh, A.,et al.: ‘A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode-clamped H-bridge cells’, IEEE Trans. Power Electron., 2011, 26, (1), pp. 51–65

16 Veenstra, M., Rufer, A.:‘Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives’, IEEE Trans. Ind. Appl., 2005, 41, (2), pp. 655–664

17 Ceglia, G., Guzman, V., Sanchez, C.,et al.: ‘A new simplified multilevel inverter topology for DC&#8211; AC conversion’,IEEE Trans. Power Electron., 2006,21, (5), pp. 1311–1319

18 Najafi, E., Yatim, A.H.M.: ‘Design and implementation of a new multilevel inverter topology’, IEEE Trans. Ind. Electron., 2012, 59, (11), pp. 4148–4154

19 Shalchi Alishah, R., Nazarpour, D., Hosseini, S.H.,et al.: ‘Novel topologies for symmetric, asymmetric, and cascade switched-diode multilevel converter with minimum number of power electronic components’, IEEE Trans. Ind. Electron., 2014,61, (10), pp. 5300–5310

20 Babaei, E., Gowgani, S.S.:‘Hybrid multilevel inverter using switched capacitor units’, IEEE Trans. Ind. Electron., 2014, 61, (9), pp. 4614–4621