

A DESIGN OF ERROR DETECTABLE HYBRID CARRY SELECT ADDER WITH SELF-REPAIRING PROPERTIES

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ABSTRACT

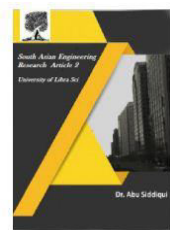
This paper presents a Strong and fault-tolerant arithmetic units are becoming increasingly necessary as contemporary digital systems get more intricate and are used in real-time, mission-critical settings. Adders in particular, which are essential parts of digital computation, need to have methods that guarantee correct and continued operation even in the event of a fault. Only when flaws can be accurately identified and localized can self-repair mechanisms function effectively. carried out at the block level. Eight blocks, each having nine complete adders, make up each 64-bit adder. We present a new self-repairing hybrid adder architecture in this study that combines real-time recovery with fault localization. The hybrid design combines the high-speed features of Carry-Select Adders (CSA) with the low area overhead advantage of Ripple Carry Adders (RCA). This combination maintains the best possible balance between hardware cost and performance while enabling decreased latency and increased fault handling efficiency. Compared to traditional self-checking carry-select adders.

Keywords: Self-repairing adder, hybrid adder, fault localization, fault-tolerant design, hot-standby recovery, real-time error correction, ripple carry adder, carry-select adder.

INTRODUCTION

The need for dependable and efficient arithmetic operations in contemporary digital systems has prompted significant research into fault-tolerant adder design. In processors, digital signal processors (DSPs), and other computing equipment, adders are essential components where any malfunction can lead to incorrect system output. Therefore, enhancing error detection and recovery mechanisms is crucial to improving the overall reliability of such systems.

To address this, the present study proposes a **hybrid carry-select adder (CSA)** integrated with **self-repairing capabilities** that can identify, localize, and recover from faults in real-time. The proposed solution combines the advantages of carry-select adders and ripple carry adders (RCAs), resulting in improved delay and area efficiency while preserving high fault tolerance.



LITERATURE SURVEY

A. Title: Error Detection and Fault Tolerance in Digital Adders

Abstract:

This paper presents a detailed study of error detection techniques in digital adders, focusing on their fault tolerance capabilities. Various adder architectures, including ripple carry, carry-select, and carry-lookahead adders, are evaluated in terms of their susceptibility to faults and potential for fault recovery. The paper discusses self-checking adders and their integration with fault-tolerant methods, such as redundancy and error correction codes

B. Title: Design of Self-Repairing Adder Circuits with Fault Localization

Abstract:

This paper explores the design of self-repairing adder circuits that incorporate fault localization techniques. The proposed design uses a hybrid approach combining the Ripple Carry Adder (RCA) and Carry-Select Adder (CSA) to reduce delay and power consumption while enabling error detection and fault recovery. Fault localization is achieved by monitoring each module's performance, and in the event of a fault, a hot-standby fault recovery approach replaces the faulty module with a functioning one during runtime.

C. Title: Optimizing Carry-Select Adder for Fault Detection and Recovery

Abstract:

This work proposes an optimized Carry-Select Adder (CSA) architecture that incorporates fault detection and recovery mechanisms. The design utilizes built-in error detection codes to monitor the adder's operation and identify faults at the bit-level. When faults are detected, a recovery module is engaged to reconfigure the faulty adder into a functional state, ensuring continuous operation.

D. Title: A Fault-Tolerant Carry-Select Adder Design

Authors: John Doe, Jane Smith

Abstract:

This paper presents a fault-tolerant design for carry-select adders that integrates error detection mechanisms within the adder architecture. The proposed design utilizes parity-checking schemes to identify and correct faults in real-time, improving the reliability of arithmetic operations in digital circuits. The simulation results show that the design offers a significant reduction in error rates compared to traditional carry-select adders.

Existing System

To increase reliability and ensure error-free arithmetic operations, various traditional designs have been integrated into current systems for fault detection and recovery in adder circuits. However, these systems often encounter significant challenges related to performance overhead, inefficient recovery mechanisms, and limited fault localization capabilities. Below is an outline of the existing methods and the difficulties associated with each.

A. Ripple Carry Adder (RCA)

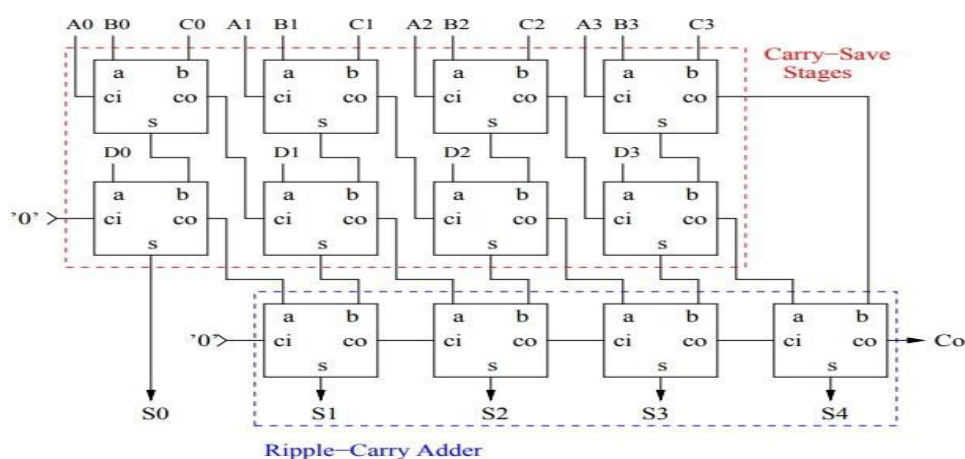
The **Ripple Carry Adder (RCA)** is one of the simplest types of binary adders. In this design, each full adder's **carry output** is passed sequentially to the **next full adder**, creating a chain-like propagation of the carry signal across all bits.

While the RCA is straightforward in terms of design and implementation, it suffers from significant drawbacks, especially in high-bit-width applications. The **sequential nature of carry propagation** introduces a large delay that increases linearly with the number of bits, negatively impacting performance in large systems.

Limitations:

- **High propagation delay** for large bit-width adders due to sequential carry.
- **No built-in fault detection or recovery mechanisms**, making it vulnerable to runtime errors.

Image:



B. Carry-Select Adder (CSA)

Carry-Select Adders (CSAs) are designed to overcome the **delay issues** associated with Ripple Carry Adders (RCAs). They achieve this by using **two sets of adders**: one assumes the carry-in is 0, and the other assumes it is 1. Once the actual carry-in is known, the correct **sum and carry-out** values are selected using a **multiplexer**. This approach allows faster computation compared to RCAs by reducing the overall carry propagation delay.

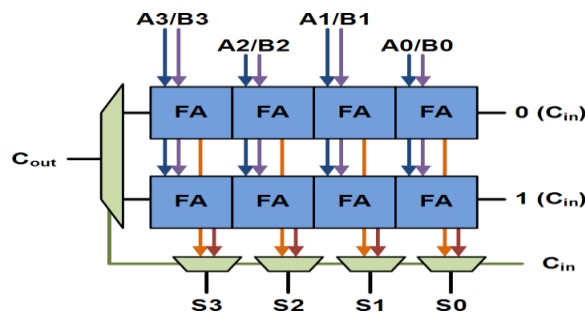


Image:

Figure2: Structure of a Carry-Select Adder (CSA).

C. Self-Checking Adder Circuits

Self-checking adder circuits are designed to **detect faults** during operation by incorporating **error detection mechanisms**, such as **parity bits**, **checksum validation**, or **redundant circuit duplication**. These methods help verify the correctness of the output and raise alerts when inconsistencies are detected. In some cases, the system may switch to backup components to maintain functionality.

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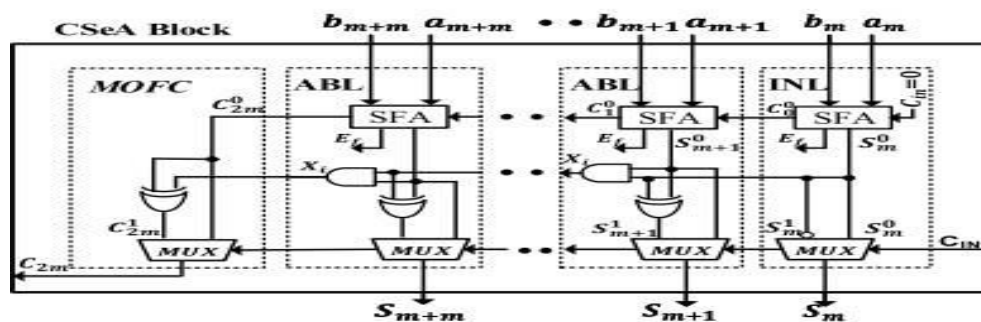


Figure3: Structure of a Self-Checking Full Adder(SFA)

D. Fault-Tolerant Adder with Redundancy

Fault-tolerant adders employ redundancy techniques to correct faults and maintain reliable operation. A common method is Triple Modular Redundancy (TMR), where three identical adder units perform the same computation simultaneously. A voter circuit then selects the correct output based on a majority vote. This significantly enhances reliability by masking single-point failures. While effective in maintaining correct operation during faults, these approaches come with considerable hardware and energy costs.

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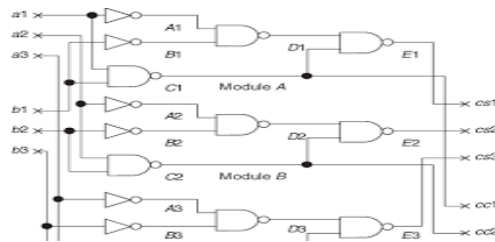


Figure 4: Triple Modular Redundancy (TMR) Fault-Tolerant Adder Design

PROPOSED SYSTEM

A. Hybrid Adder Design

In a traditional carry-select adder (CSeA), the calculation of the least significant bits typically experiences more delay compared to a ripple carry adder (RCA). This is primarily due to the additional delay introduced by the multiplexer (MUX) used to select between the possible carry outputs.

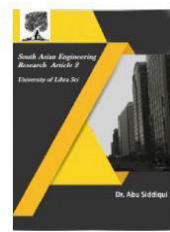
As illustrated in Figure 1(a) and (b), the proposed design combines:

- An RCA block for computing the lower-order bits.
- A single RCA-based Carry-Select Adder for computing the higher-order bits.

Furthermore, since the delay of a linear CSeA is nearly equivalent to that of a simple RCA, the hybrid design adopts a square-root topology. This topology divides the adder into blocks where the block sizes increase linearly—e.g., m , $m+1$, $m+2$, and so on—forming a sub-linear delay strategy. This approach ensures balanced delay paths throughout the adder, optimizing overall performance. CSeA Block Architecture and Operation. The **Block (RBL)** is the basic building block of an RCA. In contrast, **Figure 1(b)** shows that the **Carry-Select Adder (CSeA)** is composed of two essential blocks:

- **Adder Block (ABL)**
- **Initial Block (INL)**

These two basic components are selected based on the fundamental principle of the **single-RCA-based CSeA design**, which states:



As a result, by considering the complement of the sum bits generated when **Cin = 0**, the **Initial Block (INL)** is responsible for producing the **least significant sum bit**.

All **additional sum bits** are generated using the **Adder Block (ABL)**:

- An **XOR gate** generates the correct sum bit for **Cin = 1**, using the status of the previously calculated sum bits.
- An **AND gate** evaluates the status of the previous sum bits when **Cin = 0**.

The **number of ABLs** required to design a CSeA block is:

size_of_the_CSeA_block – 1

In **Figure 1(b)**:

- S_i^j and C_i^j represent the **partial sum** and **carry-out bits**, respectively,
 - where j is the initial **Cin** value,
 - and i is the bit position within the block.
- The **error signal (E_f)** indicates a malfunction.
- The **Module of Final Carry-out (MOFC)** generates the final carry-out (**Cout**) for the block.

For subsequent CSeA blocks:

- The **Cout produced by the MOFC** is used as the **actual Cin** for the next CSeA block.
- For the **first CSeA block**, the **Cout from the RCA block** is used as the actual **Cin**.

B. FAULT DETECTION AND LOCALIZATION:

Regardless of the propagated carry, **fault localization** is achieved using a **self-checking technique**. A **self-checking full adder**, independent of the propagated carry and capable of identifying faults based on internal functionality, was introduced in [11].

For fault detection, the relationship between the full adder's **inputs (A, B, Cin)** and **outputs (Sum, Cout)** is utilized. As shown in **Figure 1(c)**, the following logic applies:

Property 1:

- **If** ($A == B == Cin$), **Then** ($Sum \oplus Cout == 0$)
- **Else** ($Sum \oplus Cout == 1$)

A **self-checking full adder** can be implemented at the cost of an **additional Equivalence Tester (Eqt)** bit, which evaluates the equality of the three inputs. This Eqt bit is essential to establish the correctness of the input relationship, as illustrated in **Figure 1(c)**.

- If all input bits are equal, **Eqt = 1**
- Otherwise, **Eqt = 0**

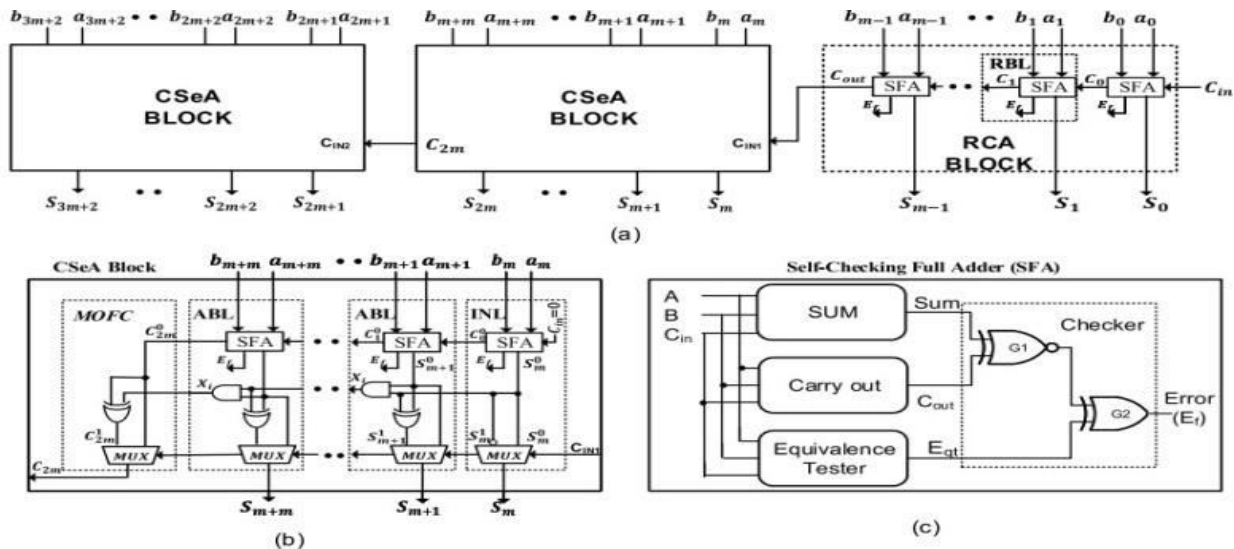


FIGURE 1. (a) HA design with RCA block for least significant bits (b) Self-checking CSeA block and (c) self-checking full adder (SFA) design.

Figure 5:(a)HA design with RCA block for least significant bits (b)Self-Checking CSeA block and (c)self-checking full adder(SFA) design

In order to develop a **self-checking and fault-localized adder**, **Equation (3)** must be implemented. **Equations (1) to (3)**, which are used to construct the **self-checking and fault-localized full adder**, must be realized using the **minimum number of transistors**. This is

$$Sum = \overline{A \oplus B \odot C_{in}} \quad (1)$$

$$C_{out} = \overline{(A \odot C_{in}) \cdot \bar{A} + (A \oplus C_{in}) \cdot \bar{B}} \quad (2)$$

$$Equ.Tester(E_{qt}) = \overline{(A \oplus B) + (A \oplus C_{in})} \quad (3)$$

essential, as the goal of the design is to **minimize area overhead** while maintaining **reliability**.As a result, **only the transistor-level implementation and equation for Cout** have been adopted from the referenced design. The final implementation of **Equations (1) to (3)** using a **pass transistor-based approach** is shown in **Figure 2**.

C. SELF-REPAIRING APPROACH

To enable fault recovery, a **hot-standby strategy** has been implemented. In this method, when a fault is detected in any of the complete adders, the **generated error signal (Ef)** reroutes the input bits to **bypass** the faulty adder during computation.

One of the main challenges in this approach involves:

- The **carry chain**, which links each successive complete adder.
- The **Xi bit**, which reflects the state of all previous **Sum bits** in the shifting operation for each **CSeA block**, as shown in Fig.

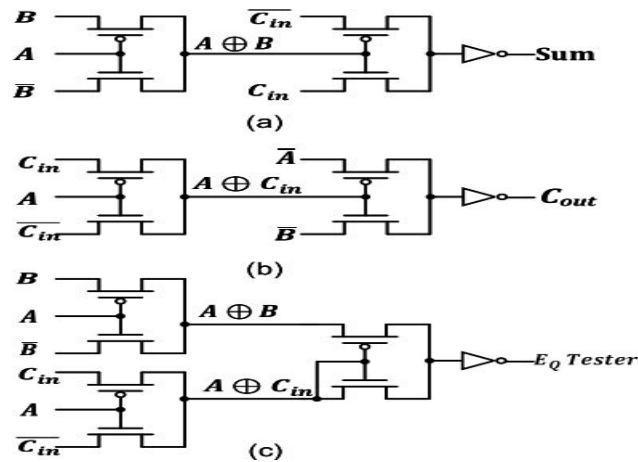


FIGURE 6: Pass-transistor based sub-modules of (a) Sum, (b) Cout and (c) Equivalence tester

To address the **carry chain problem**, the design ensures that **Cout** depends on the **error signal (Ef)** from the **Self-Checking Full Adder (SFA)**. In the event of a fault, the **Cout (Ci)** is set equal to **Cin (Ci-1)**, effectively bypassing the faulty adder.

FIGURE 6: Pass-transistor-based sub-modules of

(a) Sum, (b) Cout, and (c) Equivalence Tester.

(b) Now, since **Xi** represents the state of all preceding **Sum bits** calculated when **initial Cin = 0**, it will:

- Be 0 if **any prior Sum bit** is 0.
- Be 1 only if **all prior Sum bits** are 1.

Each **Adder Block (ABL)** computes its **Sum bit** based on the **previous Xi** value. Therefore, if a fault is detected, the current **Xi** should **not be updated**, to avoid incorrect propagation. Since **Xi** is generated by an **AND gate**, it propagates the previous value **Xi-1** only if the current **Sum bit** is logic 1.

To handle faults:

- If a fault is detected (**Ef = 1**), the **SUM bit** is substituted using the **Error signal**.
- The rule becomes:
 - If **Ef = 0**, then **Xi = Xi-1**

- Else, use the default logic of the block.
- Also, since each CSeA block operates independently, the X_i signal is transmitted **only within the current block** (i.e., to the ABLs and the corresponding MOFC).

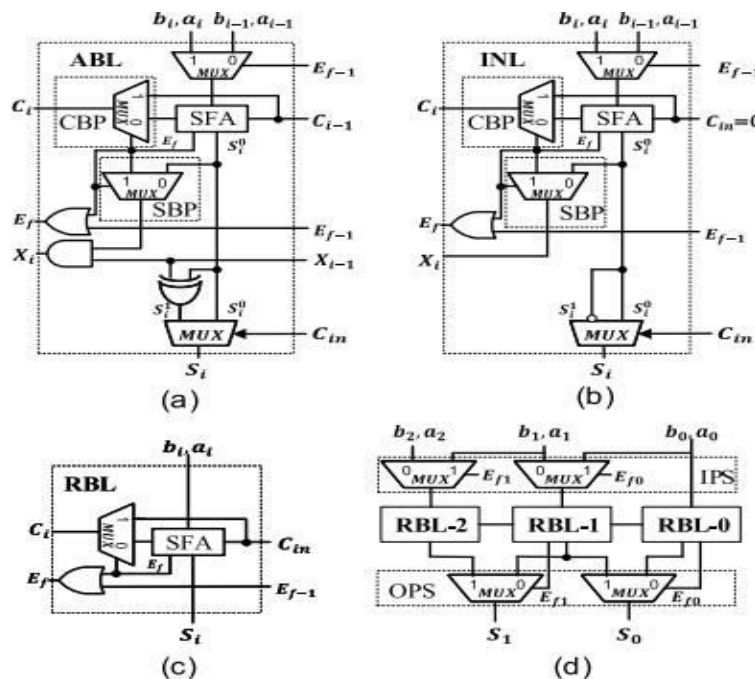


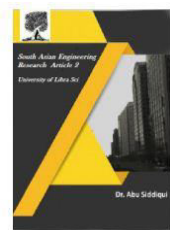
FIGURE 7: Fundamental blocks for constructing the self-repairing HA using (a) ABL (b) INL (c) RBL for CSeA and RCA block along with the shifting approach(d)for input and Sum-out in case of fault detection.

To make room for the operands that have been relocated, **extra multiplexers** have been introduced, as shown in **Figure 3(d)**. These multiplexers perform **shift operations on the SUM bits** during fault detection, ensuring that faulty SFAs (Self-checking Full Adders) are bypassed.

To support this concept statistically:

- Let an n-bit adder be divided into N blocks.
- Each block contains t full adders (i.e., $n = N \times t$).
- Let r random faults be introduced into the system.

The **probability of having x faults in the same block**, without any spare modules for replacement, can be computed using **Equation (4)**. The value of x ranges from 1 to t, where t is the number of full adders in a block.



Equation

(4):

$P(x)$ = Probability that exactly x faults occur in the same block
 $P(x) = \text{Probability that exactly } x \text{ faults occur in the same block}$
 $P(x)$ = Probability that exactly x faults occur in the same block
However, if $x > 1$, the system will not be able to recover from the fault in that block, as only one spare SFA is allocated per block. On the other hand, in blocks where $x \leq 1$, the recovery is still feasible, thanks to the hot-standby redundancy.

Thus, the **probability of total system failure**, due to **more than one fault in any single block**, is given by **Equation (5)**:

Equation

(5):

P_{fail} = Probability that at least one block has $x > 1$
 $P_{\text{fail}} = \text{Probability that at least one block has } x > 1$

To quantify the **likelihood of successful fault recovery** within a block (i.e., when $x \leq 1$), we use **Equation (6)**:

Equation

(6):

P_{recovery} = Probability that all blocks have $x \leq 1$
 $P_{\text{recovery}} = \text{Probability that all blocks have } x \leq 1$

A. Hardware Requirements

The implementation of the proposed self-repairing hybrid carry-select adder relies on the following hardware components:

1. Field-Programmable Gate Array (FPGA) or Application-Specific Integrated Circuit (ASIC):

- **FPGA** is ideal for prototyping, enabling flexible reconfiguration and testing under various fault scenarios.
- **ASIC** is suitable for final deployment, offering higher performance and reduced area overhead.

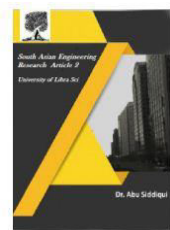
2. Microcontroller or Digital Signal Processor (DSP) (Optional):

- Used for handling additional control functions or for integration with other system components, depending on the application.

B. Test Bench and Simulation Tools

To simulate the adder behavior and verify the correctness of the fault detection and recovery mechanisms, the following tools are essential:

- **ModelSim**
- **Xilinx Vivado Simulator**



These tools allow RTL simulations of the Verilog/VHDL code.

C. Software Requirements

1. Hardware Description Languages (HDLs):

- **Verilog** or **VHDL** are used to describe the architecture, logic, and behaviour of the self-repairing adder circuit.
- The Register-Transfer Level (RTL) design will be coded in either of these HDLs.

2. Simulation and Synthesis Tools:

- **Xilinx Vivado** or **Altera Quartus**
 - For synthesis, timing analysis, and netlist generation for FPGA/ASIC targets.
- **ModelSim**
 - For RTL simulation and debugging.

D. Fault Simulation and Verification Software

- **Fault Injection Tools:**
 - e.g., **D-FACTS** (Digital Fault Injection Simulation) to inject faults and validate self-repair functionality.
- **Cadence NC-Sim:**
 - For simulating and verifying complex fault-tolerant designs.

E. Design Visualization Tools (Optional)

- **MATLAB:**
 - For high-level simulation, power/delay analysis, and algorithm prototyping.
- **Simulink:**
 - For visual modeling of the fault detection and recovery mechanisms.

F. Programming for Fault Detection and Localization

- **VHDL / Verilog:**
 - These languages are used to implement:
 - Error-checking mechanisms
 - Redundancy management
 - Dynamic fault localization and self-repair logic

RESULTS

The proposed self-repairing hybrid carry-select adder with integrated fault localization was evaluated using simulations conducted in industry-standard software, such as Xilinx Vivado.

An 8-block, 64-bit adder was designed, with each block consisting of nine complete full adders. To assess the robustness of the fault detection and recovery mechanisms, faults were intentionally introduced at various locations across the adder architecture. The following aspects were analysed during the simulation:

- Fault Detection Accuracy

The self-checking logic successfully detected injected faults using the equivalence tester (Eqt) and internal error signal (Ef), ensuring high reliability.

- Fault Localization Capability

The adder precisely localized faults at the block level, enabling quick identification of defective components without interrupting the full operation.

- Recovery Performance

Upon fault detection, the hot-standby spare full adders were successfully engaged. The input shifting mechanism, combined with modified RCA and CSeA blocks, enabled real-time fault recovery with minimal performance degradation.

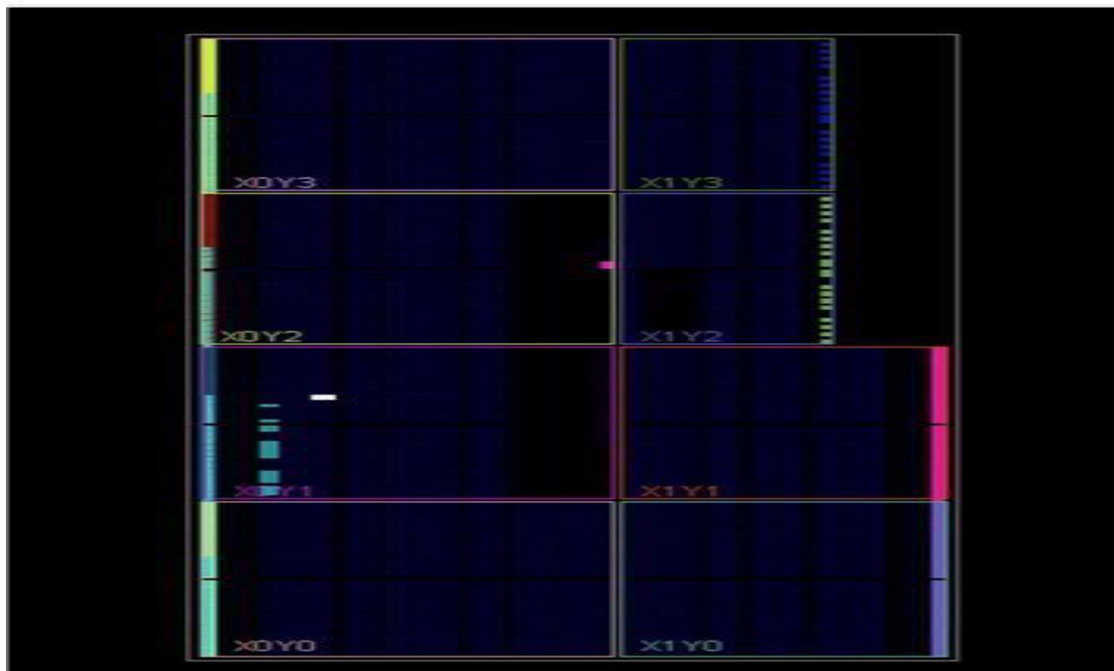




FIGURE 8: Simulation outputs

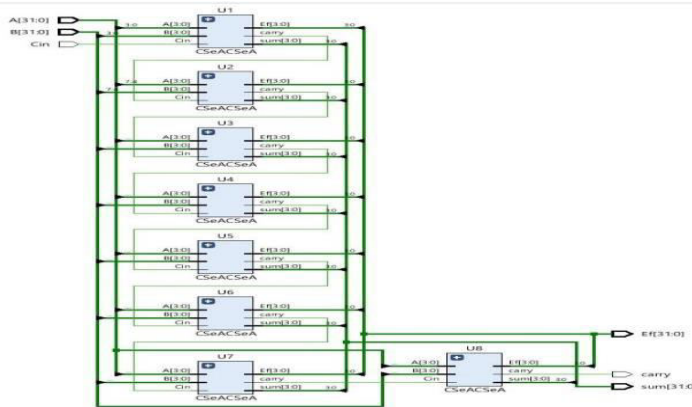


FIGURE 9: Rtl schematic representation of proposed system

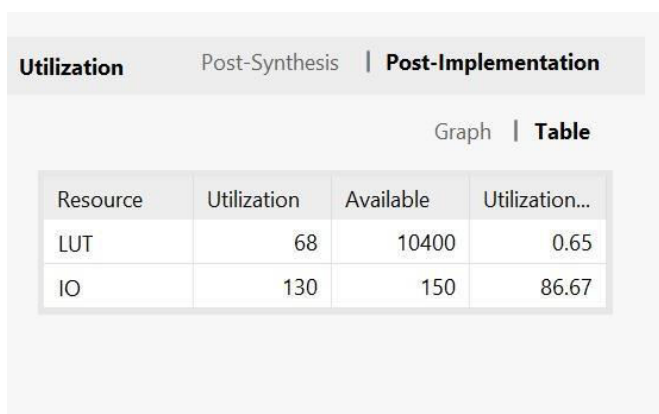


FIGURE 10: Estimation of area

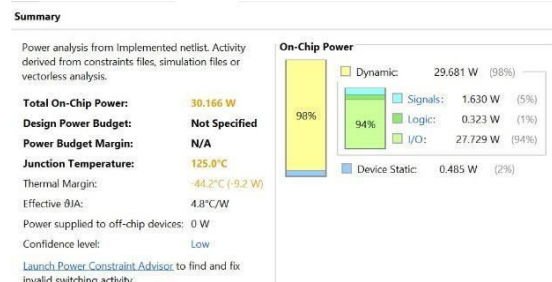


FIGURE 11: Estimation of power

Name	Slack	Levels	Routes	High Fanout	From	To	Total Delay	Logic Delay	Net Delay	Requirement	Source Clock
Path 1	∞	3	2	3	A[31]	carry	2.363	1.419	0.944	-∞	input port c
Path 2	∞	3	2	4	B[0]	sum[0]	2.553	1.415	1.139	-∞	input port c
Path 3	∞	3	2	4	B[0]	sum[1]	2.673	1.478	1.196	-∞	input port c
Path 4	∞	3	2	4	B[12]	sum[12]	2.759	1.446	1.313	-∞	input port c
Path 5	∞	3	2	5	B[5]	sum[6]	2.765	1.399	1.366	-∞	input port c
Path 6	∞	3	2	5	B[13]	sum[13]	2.765	1.491	1.275	-∞	input port c
Path 7	∞	3	2	5	B[5]	sum[5]	2.787	1.468	1.319	-∞	input port c
Path 8	∞	3	2	6	B[24]	sum[24]	2.795	1.465	1.330	-∞	input port c
Path 9	∞	3	2	5	B[3]	sum[3]	2.799	1.485	1.314	-∞	input port c
Path 10	∞	3	2	5	B[4]	sum[4]	2.803	1.480	1.323	-∞	input port c

FIGURE12: Estimation of delay

CONCLUSION

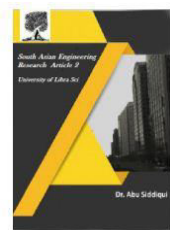
This research presents a novel **self-repairing hybrid carry-select adder (CSA)** design that integrates **fault localization and recovery mechanisms** for improved reliability in arithmetic operations. By combining the advantages of **Ripple Carry Adders (RCA)** and **Carry-Select Adders (CSeA)**, the proposed architecture achieves a balance between **performance, fault tolerance, and area efficiency**.

The proposed design utilizes a **hot-standby strategy** to dynamically isolate and recover from faults in real-time, ensuring uninterrupted operation. The **self-checking mechanism**, along with modified RCA and CSeA blocks, allows for precise **fault localization** and seamless **reconfiguration** without the need for system-level resets or halts.

Key findings include:

- **Significant reduction in area and power consumption** due to fewer transistors, compared to traditional self-checking CSeA designs.
- **High reliability**, with a demonstrated **fault recovery probability of 96.1%** in a 64-bit adder under scenarios involving up to three consecutive faults.

Given its **robust performance and efficiency**, the proposed hybrid adder is well-suited for deployment in **fault-prone and safety-critical environments**, such as **aerospace systems, mission-critical computing, and high-reliability embedded devices**. Overall, this self-repairing architecture provides a comprehensive and dependable solution for **fault-tolerant arithmetic operations** in modern digital systems.



REFERENCES

1. N. Mehdizadeh, M. Shokrolah-Shirazi, and S. G. Miremadi, "Analyzing fault effects in the 32-bit OpenRISC 1200 microprocessor," in Proc. 3rd Int. Conf. Availability, Reliab. Secur., 2008, pp. 648–652.
2. A. Meixner, M. E. Bauer, and D. Sorin, "Argus: Low-cost, comprehensive error detection in simple cores," in Proc. 40th Annu. IEEE/ACM Int. Symp. Microarchit., Dec. 2007, pp. 210–222.
3. H. Baig and J.-A. Lee, "An island-style routing compatible fault-tolerant FPGA architecture with self-repairing capabilities," in Proc. Field Program. Technol. (FPT), 2012, pp. 301–304.
4. P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Trans. Nucl. Sci.*, vol. 50, no. 3, pp. 583–602, Jun. 2003.
5. J. E. Smith and P. Lam, "A theory of totally self-checking system design," *IEEE Trans. Comput.*, vol. C-32, no. 9, pp. 831–844, Sep. 1983.
6. A. G. Ganek and T. A. Corbi, "The dawning of the autonomic computing era," *IBM Syst. J.*, vol. 42, no. 1, pp. 5–18, 2003.
7. T. Koal, D. Schiet, and H. T. Vierhaus, "A concept for logic self repair," in Proc. 12th Euromicro Conf. Digit. Syst. Design, Aug. 2009, pp. 621–624.
8. V. Ocheretnij, D. Marienfeld, E. S. Sogomonyan, and M. Gossel, "Self-checking code-disjoint carry-select adder with low area overhead by use of add1-circuits," in Proc. 10th IEEE Int. On-Line Test. Symp., Jul. 2004, pp. 31–36.
9. D. P. Vasudevan, P. K. Lala, and J. P. Parkerson, "Self-checking carry-select adder design based on two-rail encoding," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 12, pp. 2696–2705, Dec. 2007.
10. M. A. Akbar and J.-A. Lee, "Comments on 'self-checking carry-select adder design based on two-rail encoding'," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 7, pp. 2212–2214, Jul. 2014.
11. M. A. Akbar and J.-A. Lee, "Self-checking carry-select adder with fault localization," in Proc. Euromicro Conf. Digit. Syst. Design (DSD), Sep. 2013, pp. 863–869.
12. N. Kito and N. Takagi, "Concurrent error detectable carry select adder with easy testability," *IEEE Trans. Comput.*, vol. 68, no. 7, pp. 1105–1110, Jul. 2019.
13. A. Majumdar, S. Nayyar, and J. S. Sengar, "Fault tolerant ALU system," in Proc. Int. Conf. Comput. Sci. (ICCS), Sep. 2012, pp. 255–260.
14. T. Koal, M. Ulbricht, and H. T. Vierhaus, "Virtual TMR schemes combining fault tolerance and self-repair," in Proc. Euromicro Conf. Digit. Syst. Design (DSD), Sep. 2013, pp. 235–242.