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DESIGN OF HIGH SPEED ADIABATIC REVERSABLE MULTIPLIER USING UNIVERSAL SHIFT REGISTER

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ABSTARCT: In this project the design of high speed adiabatic reversible multiplier using universal shift register is proposed. The reversible logic has the promising applications in emerging computing. To generate useful gate function, reversible gates require some constant inputs. NS-Gate Multiplier is used one-to-one mapping function. At last the proposed system can shift and rotate multiple bits in a single cycle.

KEY WORDS: Reversible multiplier, NS-gate multiplier and universal shift register.

I. INTRODUCTION

In the modern time, integrated circuit (chip) is widely applied in the electronic equipment. Almost every digital appliance, like computer, camera, music player or mobile phone, has one or several chips on its circuit board. Very Large Scale Integration (VLSI), in general, comprises over an excess of one million transistors, an incredible figure that could not have been imagined a decade ago. Though the complexity of the chip has compounded by a factor of 1000 since its first introduction, yet the term VLSI still remains to be accepted and denotes digital integrated systems with high complexity. Further past few decades have witnessed an extraordinary increase in VLSI research. The Computer-Aided Design (CAD) has further aided the growth in the complexity and performance of integrated circuits in the VLSI technology. With such a phenomenal increase in complexity, it is more crucial than ever before to manage the design process, in order to maintain the reliability, quality, and extensibility of a given design. The process includes "definition, execution and control of design methodologies in a flexible and configurable way". Speed of development in high-performance computing, telecommunications and consumer electronics in a rapidly changing market, developmental costs, and cost involved in case of mistakes, play a critical role in a commercial environment. Hence, it requires designs that can be processed quickly, cheaply and mistakes brought to the forefront at the earliest, perhaps, before fabrication stage.

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Reversible logic is a promising computing design paradigm which presents a method for constructing computers that produce no heat dissipation. Reversible computing emerged as a result of the application of quantum mechanics principles towards the development of a universal computing machine. Specifically, the fundamentals of reversible computing are based on the relationship between entropy, heat transfer between molecules in a system, the probability of a quantum particle occupying a particular state at any given time, and the quantum electrodynamics between electrons when they are in dose proximity.

The basic principle of reversible computing is that a bijective device with an identical number of input and output lines will produce a computing environment where the electrodynamics of the system allow for prediction of all future states based on known past states, and the system reaches every possible state, resulting in no heat dissipation. A reversible logic gate is an N-input N-output logic device that provides one to one mapping between the input and the output. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs. Garbage outputs are those which do not contribute to the reversible logic realization of the design.

II. LITERATURE SURVEY

Conventional combinational logic circuits dissipate heat for every bit of information that is lost during their operation. Due to this fact the information once lost cannot be recovered in any way. But the same circuit if it is constructed using the reversible logic gates will allow the recovery of the information. In 1960s R. Landauer demonstrated that even with high technology circuits and systems constructed using irreversible hardware, results in energy dissipation due to information loss [1]. He showed that the loss of one bit of information dissipates KTln2 joules of energy where K is the Boltzman's constant and T is the absolute temperature at which the operation is performed [1].

Later Bennett, in 1973, showed that these KTln2 joules of energy dissipation in a circuit can be avoided if it is constructed using reversible logic circuits [2]. In reversible logic, there is a one to one mapping between inputs and outputs and for this reason no information is lost. Reversible logic is widely used in the fields of Quantum Computing, Nanotechnology, and DNA Computing etc. Different architectures of reversible barrel shifter [1], [2], [6] have been proposed in literature which can rotate at most log n bit for n-bit input. In this paper, a novel approach of reversible barrel shifter is proposed where maximum shift amount is (n − 1) bit. The proposed design performs rotation operation in both directions and it requires less number of gates, quantum cost and garbage outputs.

In 2007 Asif I. Khan, Nadia Nusrat, Samira M. Khan and Mozammel H.A. Khan [7] realized the ternary Toffoli gate and modified Fredkin gate. Realization of the quantum circuits is done using generalized ternary gates and Feynman gates then are being replaced with their equivalent

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realization using Muthukrishnan-Stroud gates. The ternary quantum gates realized by them are more efficient and have less quantum cost. In 2010 Saurabh Kotiyal, Himanshu Thapliyal and Nagarajan Ranganathan [6] propose a proficient architecture and design of a reversible ternary barrel shifter.

The ternary barrel shifter is being realized using the Modified Fredkin gates (MFG) and the ternary Feynman gates. In this they used multiple value reversible logic in order to design the (4:2) ternary barrel shifter which was being attempted first time in literature. In order to calculate the quantum cost they have used the MS-gate and shift gate which is being used in implementation of reversible barrel shifter. In this quantum cost, ancilla bits and garbage output is being calculated.

In 2012 Nayereh Hosseini Nia [2] proposed optimized (9, 2) Reversible bidirectional logical barrel shifter, optimized (6, 10) Reversible right barrel shifter & GRS-bit generation and optimized (6, 10) Reversible normalization logical left barrel shifter for floating point arithmetic for the first time in literature. The proposed optimized binary shifters are designed using Feynman gates, Fredkin gates and Peres Gates. Some parameters such as the amount of garbage outputs, the number of constant inputs, size of the circuit and quantum costs are being calculated.

III. PROPOSED SYSTEM

Conservative logic is called reversible conservative logic when there is a one-to-one mapping between the inputs and the outputs vectors along with the property that there are equal numbers of 1s in the outputs as in the inputs. Conservative logic circuits are not reversible, if one-to-one mapping between the inputs and the outputs vectors is not preserved. Conservative logic can be reversible in nature or may not be reversible in nature. Reversibility is the property of circuits in which there is one-to-one mapping between the inputs and the output vectors that is for each input vector there is a unique output vector and vice-versa. QCA is one of the emerging nanotechnologies in which it is possible to implement reversible logic gates.QCA makes it possible to achieve circuit densities and clock frequencies beyond the limits of existing CMOS technology.

In QCA, computing logic states of 1 and 0 are represented by the position of the electrons inside the QCA cell. Thus, when the bit is flipped from 1 to 0 there is no actual discharging of the capacitor as unconventional CMOS. Hence, QCA does not have to dissipate all its signal energy during transition. Further, propagation of the polarization from one cell to another is because of interaction of the electrons in adjacent QCA cells. As there is no movement of electrons from one QCA cell to the other, there is no current flow. Therefore, QCA has significant advantage compared to CMOS technology in terms of power dissipation. Due to high error rates in nano-scale manufacturing, QCA and other nanotechnologies target reducing device error rates

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Different design alternative for reversible barrel shifters that execute the following actions: logical Right shift, rotate right, shift right arithmetic, shift left arithmetic, logical left shift, and rotate left are Mux-based data reversal barrel shifters, mask-based data-reversal barrel shifters, mask-based two's complement reversible barrel shifters, and mask-based one's complement barrel shifters. On the basis of delay and area many design barrel shifters are being compared for various operand sizes and have reached the conclusion that reduction in area is being shown by data-reversal barrel shifter than one's complement barrel shifter or two's complement and reduction in amount of delay is shown by mask-based data-reversal barrel shifter than the other alternative designs.

Due to the reason zero detection and overflow of bits detection is performed in parallel with the rotation of bits or shift operation so data-reversal Mask-based barrel shifters are especially eye-catching. One more substitute design of barrel shifter is logarithmic barrel shifter. A logarithmic reversible barrel shifter consists of m number of input bits and K select lines that performs the amount of shifting of bits to be performed. The irreversible logarithmic barrel shifter has k = log2n no. of stage in order of i=0, 1, …, (K–1).In each and every step if control bit signal di is equal to 1 after that 2i time bit shifting operation is being performed on input bits or else the input bits shall not be altered. Using 2×1 multiplexers the irreversible logarithmic shifter is being realized.

The unidirectional barrel shifter is being designed by means of quantum Modified Fredkin gates (MFG), quantum ternary Feynman gates (TFG) and modified ternary Peres gates (TPG). The modified unidirectional barrel shifter can only shift the input bits to left. A four bit modified unidirectional barrel shifter has two stages (ki, i = 0, 1). In this proposed ternary barrel shifter the TPG at the input is being replaced by modified peres gate which performs the same function but its MS gate complexity is reduced. The total numbers of quantum gates being used to implement modified unibarrelshifter are 198 and no. of garbage outputs being produced are 3. Proposed Uni-barrel shifter can only perform as left shifter. According to the values of (k0,k1) the uni-barrel shifter performs the shift of bits . As the value of control bit changes the amount of shift also changes as if value of control bit is 00 than no shift will be performed but if control bit is assigned 01 value than the input bits will get shifted to left by one bit

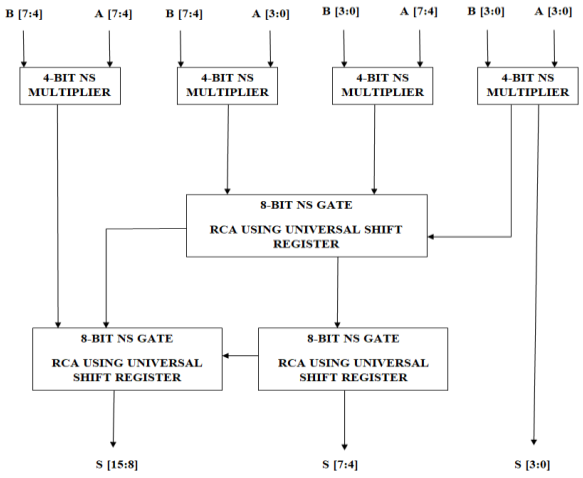

Fig. 1: PROPOSED SYSTEM

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SHIFTER UNIT: The shifter unit in the design of reversible bidirectional arithmetic and logical shifter is responsible for the amount of shift operation performed. This unit is controlled by the control signals S2, S1 and S0. The shifter unit can be divided into three stages. All the three stages are designed using the chain of 8 Fredkin gates controlled by the control signals S2, S1 and S0. The first, second and the third stages of the shifter unit right shifts the input data by 22, 21 and 20 bits depending on the value of control signal S2, S1 and S0, respectively. The three stage design of the reversible shifter unit. The Feynman gates are used in the design to avoid the fan out problem. The working of the three stages of the shifter unit is explained as follows:

• **Stage-1:** The first stage of shifter unit is responsible for shifting the input data by 2 2 -bits and is controlled by the control signal S2. If the value of control signal S2 is 1 the input data is right shifted by 22 -bits, else the input data remains unchanged. The outputs of the Stage 1is passed as inputs to Stage 2 of the shifter unit.

• **Stage-2:** The second stage of the shifter unit works on the outputs of the first stage and is controlled by the control signal S1. If the value of control signal S1 is 1 the input data provided to the second stage is right shifted by 21 -bits, else the input data remains unchanged. The outputs of the Stage 2 are passed as inputs to Stage 3 of the shifter unit.

• **Stage-3:** The third stage of the shifter unit is controlled by the control signal S0. If the value of control signal S0 is 1 the output data generated by the stage-2 is right shifted by 20 -bits else the output data remains unchanged. The outputs of this stage are passed as inputs to the next module in the design of reversible bidirectional arithmetic and logical shifter.

NS-Gate

The figure shows the NS gate. NS gate can perceive all Boolean logical operators. The input is pattern analogous to a particular output pattern. The both input and output bits are taken in parallel. The most noteworthy, considerable attribute of the proposed gate is that it can work individually as a reversible full adder, reversible full subtractor, reversible half adder, and reversible half subtractor. That is now we are capable of implementing reversible full adder, subtractor and reversible half adder, subtractor with a single gate only. The proposition of this meticulous manuscript is a design a parity preservation property using NS Gate.

IV. RESULTS

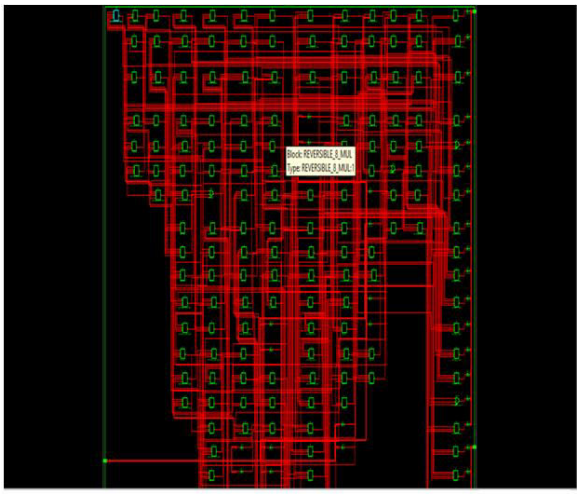

Fig. 2: SCHAMATIC OF PROPOSED SYSTEM

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Fig.3: OUTPUT WAVEFORM

V. CONCLUSION

An approach to realize the shift register was presented in this paper which consumes less power and the less no. of gates in its implementation. The functional verification of the proposed design of the reversible shift register is performed through simulations using the Verilog HDL flow for reversible circuits. The proposed design can perform logical right shifting, arithmetic right shifting, rotating right, logical left shifting, arithmetic left shifting and rotating left operations. Hence this gives effective results.

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