**AN EFFICIENT IMPLEMENTATION OF DC-LINK VOLTAGE CONTROL STRATEGY FOR GRID CONNECTED CONVERTERS**

**#1 M.V.V. SURESH, #2D.RAMESH BABU**

1M.TECH STUDENT, DEPARTMENT OF EEE, KAKINADA INSTITUTE OF TECHNOLOGICAL SCIENCES (KITS), RAMACHANDRAPURAM

2ASSISTANT PROFESSOR, DEPARTMENT OF EEE, KAKINADA INSTITUTE OF TECHNOLOGICAL SCIENCES (KITS), RAMACHANDRAPURAM.

# Abstract: This paper presents a robust control strategy to improve dc-link voltage control performances for Grid connected Converters (GcCs). The proposed control strategy is based on an adaptive PI controller and is aimed to ensure fast transient response, low dc-link voltage fluctuations, low grid current THD and good disturbance rejection after sudden changes of the active power drawn by the GcC. The proportional and integral gains of the considered adaptive PI controller are self-tuned so that they are well suited with regard to the operating point of the controlled system and/or its state. Several simulation and experimental results are presented to confirm and validate the effectiveness and feasibility of the proposed dc-link voltage control strategy.

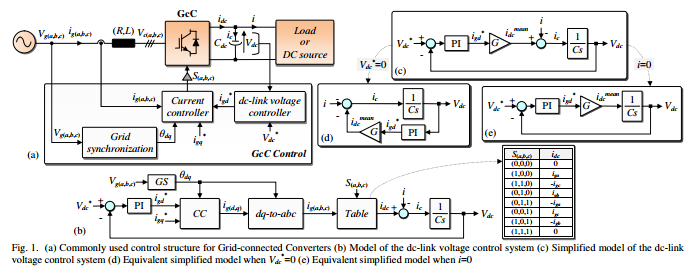
**Index Terms** - DC-link voltage control, adaptive PI controller, Grid connected Converters

1. **INTRODUCTION**

SINGLE-PHASE Grid connected Converters (GcCs) play a key role in applications like renewable energy systems [1] and modern rectifiers [2-3] due to their ability to deliver the required DC-link voltage level with the possibly highest grid current quality by means of improved control techniques [4]. A passive element called DC-link is generally used in the dcside of the converter to supply the DC power demand. This element is generally capacitive and decouples the power pulsation between the DC and AC sides of the converter. The difficulties in controlling single-phase GcCs arise from two issues. The first one is related to fluctuations in the DC-link voltage mainly caused by sudden changes of the active power drawn by the single-phase GcC. These fluctuations must be within limits constrained by the voltage rating of both the DClink voltage capacitor and the converter power switches. The second issue is related to the low frequency components of the DC-link voltage ripples that oscillate at twice the grid frequency. These ripples are typical features of single phase AC systems and are caused by the 2f oscillation of the transferred active power [5-6]. The measurement of these ripples in a control loop will result in a distorted grid current reference that will cause additional harmonic components in the grid current [7]. So, the control objectives pertaining the DC-link voltage controller of a single-phase GcC can be summarized as follows: 1) The average value of the DC-link voltage must track its reference with zero steady state error; 2) The fluctuations of the DC-link voltage should be minimized after sudden changes of the active power drawn by the converter; and 3) The grid current must be prevented from additional harmonic contents. It should be noted here that the two aforementioned objectives constitute a trade-off for the design of standard PI controllers. There are several converters topologies for single-phase GcCs[8]. Fig.1 shows a commonly used half-bridge converter topology along with its controller for single-phase GcCs. Depending on the considered application, the DC-side terminals can be connected to either a power source or an electrical load. The controller is composed of three main functions:1) The grid synchronization (GS) function [9] that generates a per unit signal ig pu synchronized with the grid voltage Vg; 2) The DC-link voltage controller (Vdc controller) that controls the DC-link voltage Vdc so that its average value is equal to its reference Vdc \* ; and 3) the current controller that controls the grid current ig so that it tracks with good accuracy its reference ig \* , which is computed by multiplying the Vdc controller output signal Igm \* by the per unit signal ig pu.

As regards the DC-link voltage controller, different control techniques were presented and discussed in the literature. The most frequently used ones are based on a standard PI controller with constant proportional and integral gains. Different PI controller design techniques were described in literature [10], but most of them do not take into account the effect of the PI controller gains on the grid current harmonics. In [11], a method for the design of the DC-link voltage controller gains that have control over the grid current harmonics as well as the DC-link voltage fluctuations is presented. However, despite that this method presents a good compromise for the two aforementioned control objectives, it can’t ensure them optimally. Others works associated PI controllers with the feed forward of the DC load (or source) current [12-13]. Although such a feed-forward solution allows efficient reduction of the DC-link voltage fluctuations, it increases the coupling between the DC and AC sides of the single-phase GcC. Thus, any noise or fast oscillation at the DC load (or source) current can create harmonics at the grid current reference signal computed via the DC-link voltage controller. An adaptive PI controller for the DC-link voltage control is presented in [14]. But this work was performed for three-phase balanced GcCs, which are not affected by the 2f oscillation of the active power thanks to symmetry of the three-phase oscillating powers. Also, it was only aimed to reduce the bus voltage fluctuations without investigating the effect of the used adaptive PI controller on the grid current harmonics. The cancellation of the 2f ripples was also achieved in [16] and [17] using notch filter tuned at twice the grid frequency. This method can ensure efficient elimination of the 2f ripples but it leads to slower transient response with a lower control bandwidth. The elimination of the 2f ripples can also be realized using active decoupling techniques as explained in [18] and [19]. These techniques require on the other hand the addition of extra controlled power circuits in the DC side, which are employed to derive the 2f ripples to another specific energy storage system. Finally, notice that fractional order PI controllers are interesting and robust controllers that need to be considered. References [20-23] demonstrated that fractional order PI controllers outperform integer order ones. Nevertheless, this is the case of integer order PI controllers with constant gains. Also, the optimizations methods presented in literature for the design of fractional order PI controllers do not consider the control objective of grid current THD reduction.

This paper presents a systematic and efficient method to design an adaptive PI controller for the DC-link voltage control of single-phase GcCs. The proportional and integral gains of the proposed controller are self-tuned according to the operating point of the controlled system and/or its state (i.e. transient or steady state) so that the DC-link voltage controller ensures at the same time reduced DC-link voltage fluctuations and reduced grid current harmonics. The rest of the paper is organized as follow. Section II presents the modeling and analysis of the DC-link voltage control loop. After that, the designed adaptive PI controller is presented in section III. Then, section IV presents and discusses the obtained experimental results. Finally, the last section summarizes the main conclusions related to this work.



**II. MODELING, DESIGN AND ANALYSIS OF THE DC-LINK VOLTAGE CONTROLLER**

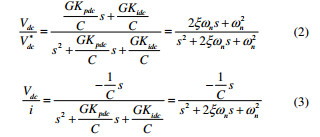
1. **Modeling and design of the dc-link voltage controller**

The studied system is depicted on Fig.1.a, where L (respectively R) is the filter inductor (respectively the filter resistor); C is the capacitor of the dc-link; Vg(a,b,c) refer to the components of the grid voltage vector in the natural reference frame; ig(a,b,c) refer to the components of the grid current vector in the natural reference frame; S(a,b,c) are the GcC switching states; Vdc is the dc-link voltage; Vdc \* is the dc-link voltage reference; idc is the current coming out from the power converter; ic is the current flowing into the capacitor C; i is the current consumed/generated by the load/the DC source connected to the dc-link; and ig(d,q) \* are the d and q components of the grid current reference in the synchronous reference frame (d,q), where the d axis is linked to the grid voltage vector. Fig.1.a shows also that the control structure of a GcC includes three main functions: the grid synchronization [21], the current controller [22] and the dc-link voltage controller [11]. Fig.1.b shows the model of the dc-link voltage control system. In this figure, GS and CC stand for grid synchronization and current controller, respectively. It can be noted that the dc-link voltage control is not in the form of a LTI system. This is mainly due to nonlinearities introduced by the idc table that computes idc current based on grid currents ig(a,b,c) and applied switching signals S(a,b,c) . To simplify the model, the relationship between the mean value of idc (idc mean) and igd \* currents is firstly determined. This relationship is deduced according to equation (1) [20]. In this equation, PAC is the active power fed in the AC side of the GcC, Vgm is the magnitude of the phase voltage, igd is the d component of the grid current and PDC is the active power fed in the DC side of the GcC. Supposing that Vdc≈Vdc \* and neglecting the power losses on the GcC and on the internal resistor of the inductive filter (PAC≈PDC), the relationship between idc mean and igd \* currents can be deduced as shown in equation (1).

****

For a simplest, but reasonably accurate modeling of the dclink voltage control, the simplified model given by Fig.1.c is considered. This simplified model is based the following assumptions: 1) the dynamic of CC loop is very fast with regard to that of the dc-link voltage control loop and 2) the nonlinearities are neglected. According to Fig.1.c, the dc-link voltage controller has two inputs: 1) the dc-link voltage reference Vdc \* and 2) the input current i. To study the dc-link voltage control loop, the superposition method is considered. Using this method and supposing that the PI controller transfer function is equal to (Kpdc+Kidc/s), two systems are derived from Fig.1.c. For the first

system (Fig.1.d and equation (2)), i is neglected, while Vdc \* is considered as an input. For the. second system (Fig.1.e and equation (3)), i is considered as an input, while Vdc \* is neglected.



Identifying denominators of (2) and (3), we deduce that 2ξωn=GKpdc/C and ωn 2 =GKidc/C, where ξ is the damping ratio and ωn is the natural frequency of oscillation. The poles p(1,2) of the transfer functions given by (2) and (3) are equal to -ξωn±jωn√(1-ξ 2 ) for 0≤ξ≤1. So, the system stability is guarantee whenever (4) is verified.

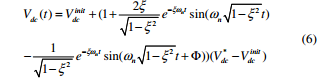


The standard PI controller can be designed using the pole placement method as in (5).

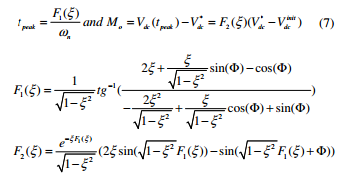


1. **Analysis of the dc-link voltage controller**

- Analysis of the dynamic response to a step jump of Vdc \* Based on equation (2), when a step jump is applied to the dc-link voltage reference value Vdc \* , the response of the dclink voltage Vdc (initially equal to Vdc init) is expressed according to (6) (with Φ = cos-1(ξ)).



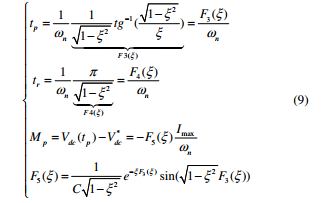
The peak time tpeak and the maximum overshoot value Mo of the dc-link voltage are deduced by solving (dVdc(t)/dt=0 for equation (6)) and are given by equation (7). 1

According to equation (7), for a fixed value of ξ and after step jumps of the dc-link voltage reference Vdc \* , better dynamic performances and shorter transient times are obtained when ωn increases. However, ωn have no effect on the obtained maximum overshoot value Mo, which depends only on the selected value for the damping ratio ξ.

- Analysis of the dynamic response to a step jump of i

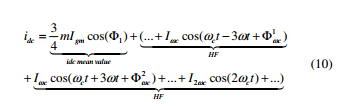
In the following, we suppose that the maximum active power Pmax generated/consumed by the DC source/Load connected to the dc-bus is known. Consequently, the maximum value Imax of the input current i is equal to Imax=Pmax/Vdc \* . Note that technical literature traditionally neglects the instantaneous power of the L filters since it is constant during steady state operation for the case of three phase GcCs. However, in rectifying mode and according to [30], the increase of the maximum value Imax will result in variation in the instantaneous power of the L filters and can lead to instability problems. That’s why, the maximum current Imax is supposed lower than a limit current that can cause unstable operation of the system. Based on equation (3), the response to a step jump of the input current i from 0 to Imax is expressed as follows

The peak time tp, after a step jump of the input current i, can be computed by solving (dVdc(t)/dt=0 for equation (8)). The response time tr (necessary for Vdc to reach again its reference Vdc \* ) can be approximately deduced from (8). The times tp and tr and the maximum overshoot value Mp are expressed according to (9).



According to equation (9), for a fixed value of ξ, better dynamic performances and lower maximum overshoot value Mp are obtained after step jumps of input current i when ωn increases.

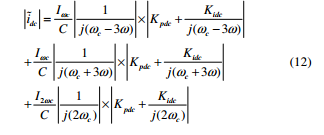
**C. Analysis of the grid current harmonics**

To derive the relationship between the output current harmonics and the selected (ξ,ωn) values, it shall be noticed that the grid current harmonics are affected by the ripples that may exist in the dc-link voltage controller output signal. These ripples are the result of the oscillating nature of the idc current. To simplify the study, let consider the case when the GcC operates with a constant switching frequency fc . For that case, and according to [28], the dc-link current can be expressed according to equation (10).

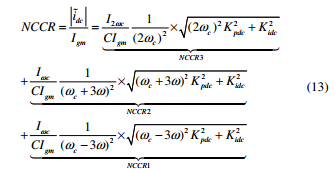
Where Φ1, Φωc 1 and Φωc 2 are constant phase angles, m is the modulation index, ω=2πf=2π50 rad/s is the frequency of the grid currents, ωc=2πfc is the switching frequency, Igm is the grid current magnitude, Iωc and I2ωc are the magnitudes of the main harmonic components (i.e. for the frequencies equal to ωc±3ω and 2ωc , respectively). Note that Iωc and I2ωc are proportional to the grid current magnitude Igm with a coefficient that depends on the used modulation index m [28]. The pulsating current idc passes through the 1/(Cs) bloc to create the bus-voltage ripples. The main dc-link voltage ripples are then equal to



The magnitude of the dc-link current ripples on the PI controller output signal can be deduced from (11) as follows



A normalized current ripple ratio NCRR is defined and computed according to (13).



Given that Iωc and I2ωc are proportional to the grid current magnitude Igm [28] (with a coefficient that depends on the applied modulation index m), the NCCR depends on the used capacitor, the used switching frequency, the used modulation index m and the selected gains Kpdc and Kidc for the PI controller. The ripples around the switching frequency in the dq synchronous reference frame (i.e. respectively (fc-3f), (fc+3f) and 2fc) become respectively (fc-2f), (fc+4f) and (2fc+f) ripples in the natural reference frame. Assuming that Hcc(s) is the closed-loop transfer function of the internal current control loop, the grid current will have harmonic content with a magnitude equal to NCCR1×|Hcc(j(ωc-2ω))|+NCCR2\*|Hcc(j(ωc+4ω))| + NCCR3×|Hcc(j(2ωc+ω))|. This harmonic content will influence the grid current THD especially for low dc bus capacitor values, low switching frequency values and high selected Kpdc and Kidc gains (when ωn increases). For the case of variable switching frequency, it is difficult to derive the main harmonic content of the dc-link voltage. However, for a given main harmonic content, the grid current THD is influenced in the same manner as the case of a constant switching frequency operation.

**III. DESIGN OF THE PROPOSED ADAPTIVE PI CONTROLLER**

The selection of the damping ratio ξ depends on the following constraints: 1) when ξ increases, the system is over damped and lower dynamic response is obtained and 2) when ξ decreases and becomes close to zero, this will result in oscillatory response. To simplify the study and to ensure a good compromise between the above mentioned constraints, the damping ratio was set to 0.7. Regarding the ωn value, it is selected according to the adaptive process described by the flow chart depicted on Fig.3.a. According to Fig.3.b, two bands are defined around the DC-link voltage reference Vdc \* : 1) an internal band which is bounded by ±Ṽdc max (where Ṽdc max =Imax/(2Cω) is the DC-link voltage ripples magnitude at maximum power) and 2) an external band limited to Vdc \* ±λVdc \* . Based on Fig.3.a, the ωn value is selected as follows

- When the instantaneous DC-link voltage Vdc is inside the internal band (|∆Vdc|≤Ṽdc max), a constant value of ωn equal to ωn min is selected. - When the instantaneous DC-link voltage Vdc is outside the external band (|∆Vdc|≥λVdc \* ), a constant value of ωn equal to ωn max is selected. - When the instantaneous DC-link voltage Vdc is inside the region delimited by the internal and external band (Ṽdc max<|∆Vdc|\* ), the selected ωn value depend on the module of the DC-link voltage error and is equal to a[Log(|∆Vdc|-Ṽdc max+1)]+b.

The coefficients a and b are constants and are respectively equal to (ωn max -ωn min)/Log(λVdc \* -Ṽdc max+1) and ωn min .

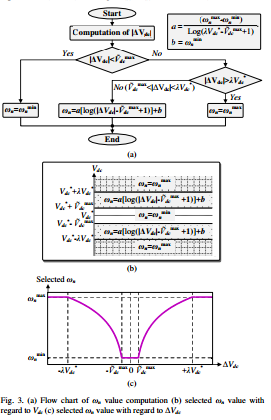


Fig.3.c shows the resulting waveform of the selected ωn value with regard to the DC-link voltage error ∆Vdc. According to this figure, the proposed adaptive process increases the selected ωn value when |∆Vdc| increases during transient states in order to reduce DC-link voltage fluctuations after step jumps of the input current i. Conversely, during steady states, when |∆Vdc| is lower than Ṽdc max, the selected ωn value is equal to ωn min to ensure lower grid current THD. The parameters λ, ωn min and ωn max are determined according to the following steps and given the maximum active power PDC max and the DC-link voltage reference Vdc.

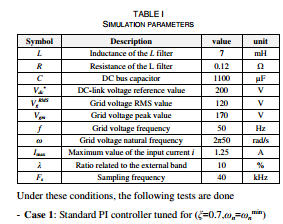
• Step 1 (Selection of λ): The voltage rating of the single phase GcC power switches and of the DC-link capacitor is determined for dynamic conditions using a suitable safety factor. Usually, 10% of Vdc \* is tolerable for dynamic conditions. For this reason, the external band limit was imposed equal to ±10%Vdc \* by selecting λ=0.1. • Step 2 (Selection of ωn max): The poles of the transfer function given by (3) are located at p(1,2)=-ξωn±j√(1-ξ 2 )ωn. The time constant of the DC-link voltage control loop is equal to τVdc=|1/Re(p(1,2))|=1/(ξωn). Supposing that the current control loop has a time constant equal to τig, the time constant τVdc must be at least ten times greater than τig. So, the ωn max value can be deduced as follows

In this work, the used current controller is based on the delta modulation (DM) technique [15] and the obtained time constant τig is lower than 1ms. Therefore, the time constant τVdc must be greater than 10ms. According to equation (10) and for a damping ration ξ equal to 0.7, ωn max is equal to1/(0.7×10ms)=143rad/s. • Step 3 (Selection of ωn min): The ωn min value should be selected so that the current distortion due to the third harmonic component h3 remains negligible. Supposing that |CC(j3ω)|≈1 and based on equations (8) and (9), the ωn min value can be computed according to a predefined h3 value as follows



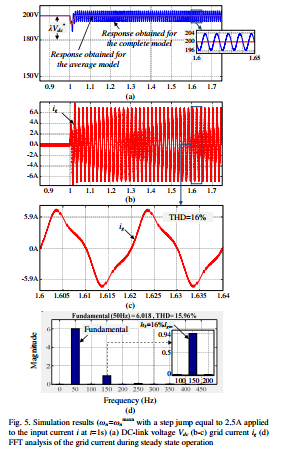
For a third harmonic component h3 limited to 2.5% and based on equation (11), ωn min is set to 22.43 rad/s. In others words, when the proportional and integral gains of the PI controller are computed according to equation (2) for ωn equal to ωn min , the resulting third harmonic component of the grid current ig will be negligible and only equal to 2.5%. Simulations are firstly done to verify the obtained theoretical results and to compare the performances of the proposed adaptive PI controller with regard to those of a standard PI controller. Notice that simulations are done based on a complete model that comprises all nonlinearities and all control loops. Tab.I summarizes the used simulation parameters. The maximum value of the input current i (related to a maximum active power PDC max) is supposed equal to 2.5A. A maximum step jump of the input current i, from 0 to Imax, is applied at t=1s. Since the mean value of the capacitor current ic is equal to zero, the magnitude of the mean value of the idc current (Idc mean) is equal to the magnitude of the mean value of the input current i. Therefore, Idc mean is equal to

2.5A during steady state and after the step jump of the input current i. Based on equation (1), the magnitude of the fundamental of the grid current ig is equal to Igm=Idc mean/G=Imax×2×Vdc \* /Vgm =5.9A. According to equation (6), the DC-link voltage ripples magnitude at maximum power is equal to Ṽdc max=3.62V.

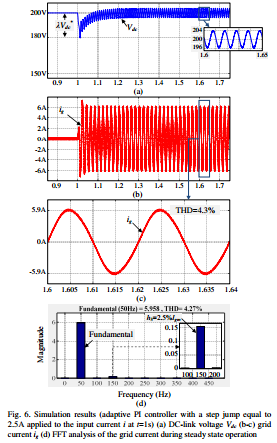


For that case, and according to equation (5), the maximum DC-link voltage fluctuation ∆Vdc max is equal to 47V, which is greater than the tolerable limit of the external band (±10%Vdc \* =±20V). Using equation (8), the normalized ratio

for the current ripples N is equal to 0.05. This means that the reference current ig \* will have a third harmonic component with a magnitude equal to 2.5%. Fig.4 presents the obtained simulation results for the first case. Simulations given by Fig.4.a show that there is a slight difference between Vdc responses obtained with the complete and average models. This can be explained by the fact the transfer function of the average model given by equation (3) supposes that the DClink voltage Vdc is approximately equal to its reference Vdc \* and that therefore the gain G defined by equation (1) is constant. As a result, a slight error is observed between ∆Vdc max computed analytically and ∆Vdc max obtained through simulation of the complete model. This being said, the highest DC-link voltage fluctuation is still obtained when the PI controller gains are tuned for ωn=ωn min. On the other hand, a negligible h3 component is obtained for the grid current and simulation results given by Fig.4.b, Fig.4.c and Fig.4.d show that the resulting grid current THD is around 4.3%. - Case 2: Standard PI controller tuned for (ξ=0.7,ωn=ωn max) For that case, and according to equation (5), the maximum DC-link voltage fluctuation ∆Vdc max is about 8V.



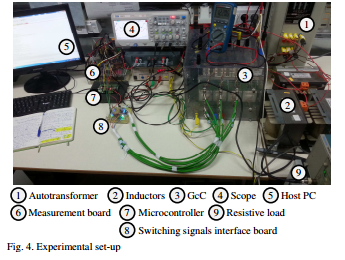
According to equation (8) of the revised manuscript, the normalized ratio for the current ripples N is equal to 32.28%. This means that the reference current ig \* will have a third harmonic component h3 with a magnitude equal to 16.14%. Fig.5 shows the obtained simulation results for the second case. It can be noted that these simulation results comply with the analytical ones. Since the |Hcc(j3ω)| is closely equal to unity and the high frequency components of the grid current are negligible with regard to the third harmonic component, the resulting grid current THD is about 16%. - Case 3: The proposed adaptive PI controller Fig.6 presents the obtained simulation results with the proposed adaptive PI controller. These results show that, the maximum DC-link voltage fluctuation is about 11V and is close to that obtained with a standard PI controller tuned for ωn=ωn max. On the other hand, the grid current THD is equal to 4.3% and is of the same order of that obtained with a standard PI controller tuned for ωn=ωn min .



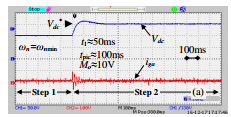
It shall be noticed that, for all the considered cases, the mean value of the DC-link voltage Vdc mean tracks with good accuracy the reference Vdc \* during steady state operation.

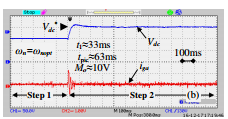
**IV. EXPERIMENTAL RESULTS**

In order to verify the efficiency of the proposed controller, the prototyping platform presented on Fig. 4 was developed. It includes three parts. The first one is a power part, which is composed of: 1) a three-phase autotransformer used to impose the desired grid voltage peak magnitude; 2) a three-phase inductive filter L; 3) a three-phase GcC; 4) a DC-link capacitor C; and 5) a resistive load ZLoad. The second one is the control part composed of 1) the STM32F4-Discovery digital solution and 2) a Host PC. Note that the used digital solution is based on Cortex-M4-ARM processor, which is associated to a Floating Point Unit (FPU) and have a system clock frequency equal to 168 MHz. Finally, the third part is an interface part that includes:1) a measurement board used to acquire seven analog measurements (Vg(a,b,c), ig(a,b,c) and Vdc) and 2) an interface board used to amplify the computed switching signals S(a,b,c). The used parameters for the experimental tests are the same as the ones presented in Tab.1



In order to eliminate noises in the measured dc-link voltage, equation (15) was implemented with a small modification. The selected ωn[k] value during a k th sampling period is computed by replacing |∆Vdc[k]| in (15) by |∆Vdc|min[k], which is equal to the minimal value of (|∆Vdc(j)|j=(k-n+1…k) (n was set to 5 for efficient elimination of the noises). The experimental tests were done according to the following steps: - Step 1: The GcC switching signals were all tied at a low logical level. For that case, the GcC works as a simple threephase diode bridge rectifier and the capacitor charge was initially set to 100V by acting on the ratio of the autotransformer. Also, the load Zload was disconnected. - Step 2: The switching signals S(a,b,c) were applied to the GcC and a step jump equal to 150V is applied to the dc-link voltage reference Vdc \* . The experimental results related to step 1 and 2 are presented in Fig.5.a, Fig.5.b and Fig.5.c. These figures compare between three cases: 1) a standard PI controller tuned for ωn=ωnmin (Fig.5.a), 2) a standard PI controller tuned for ωn=ωnopt (Fig.5.b) and 3) the proposed controller (Fig.5.c). It can be noted that the proposed controller ensures a dc-link voltage step response with good dynamic performances and without overshoot during the first transient states..

****

****

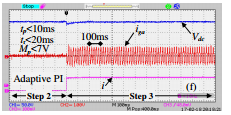
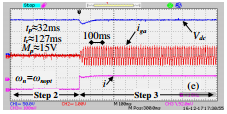
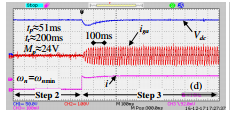
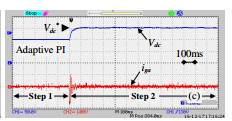
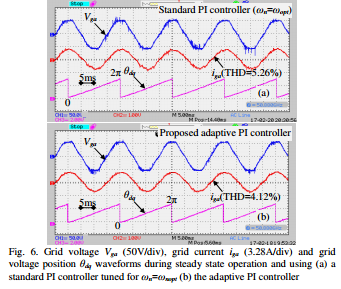


Fig. 5. (a-b-c) DC-link voltage Vdc (50V/div) and grid current iga (3.28A/div) waveforms during steps 1 and 2 (a) Standard PI controller (ωn=ωnmin) (b) Standard PI controller (ωn=ωnopt) (c) Proposed adaptive PI controller (e-f-g) DC-link voltage Vdc (50V/div) and grid current iga (3.28A/div) waveforms during steps 2 and 3 (e) Standard PI controller (ωn=ωnmin) (f) Standard PI controller (ωn=ωnopt) (g) Proposed adaptive PI controller

- Step 3: As explained previously, the proposed method supposes that the input current will not exceed a predefined maximum value Imax. The worst case that will lead to a maximum overshoot value Mp is a sudden and sever change of the input current i that can be approximated to a step jump from 0 to Imax (for a sudden maximum power load connection). For others kinds of loads, characterized by a smoother input current i change, the overshoot will be lower than the considered worst case. During step 3, the control performances in terms of disturbance rejection were tested through a sudden connection of a resistive load ZLoad equal to Vdc \* /Imax=150V/1.25A=120Ω. The experimental results related to steps 2 and 3 are presented in Fig.5.d, Fig.5.e and Fig.5.f. These figures compare between three cases: 1) a standard PI controller tuned for ωn=ωnmin (Fig.5.d), 2) a standard PI controller tuned for ωn=ωnopt (Fig.5.e) and 3) the proposed controller (Fig.5.f). It can be noticed that the input current i response can be approximated to a step jump from 0 to Imax and that the obtained experimental results are quite close to those obtained in simulation results shown in Fig.3.



Finally, Fig.6 shows the grid voltage Vga waveform with regard to the grid current iga and the estimated θdq position waveforms during steady state operation for a standard PI controller tuned for ωn=ωnopt (Fig.6.a) and for the proposed adaptive PI controller (Fig.6.b). This figure shows that a unitary power factor operation was achieved for both cases. Also, the use of the adaptive PI controller allowed the reduction of the grid current THD (the THD was reduced from 5.26% for the case of a standard PI controller to 4.12% for the proposed controller).

**V. CONCLUSION**

This paper presented a DC-link voltage control for single phase GcCs using an adaptive PI controller. The PI controller gains are continuously updated through the selection of the natural frequency ωn related to the transfer function from the input current i to the DC-link voltage Vdc. The interactions between the selected ωn value (on one hand) and the DC-link voltage fluctuations in addition to the introduction of a third harmonic component on the grid current (on the other hand) are formulated and quantified. The main purpose of the proposed control is to solve the trade-off that exists between tow control objectives: 1) minimization of DC-link voltage fluctuation and 2) minimization of grid current THD. For this, the ωn value is selected using an adaptive process that ensures an efficient reduction of the DC-link voltage fluctuation during transient state operation without affecting grid current THD during steady state operation. Simulation and experimental results confirm the effectiveness of the proposed DC-link voltage controller.

**REFERENCES**

[1] D. Casadei, M. Mengoni, G. Serra, A. Tani, and L. Zarri, “A control scheme with energy saving and dc-link overvoltage rejection for induction motor drives of electric vehicles,” IEEE Trans. Ind. Appl., vol. 46, no. 4, pp. 1436–1446, Jul./Aug. 2010. [2] Li, F., Zou, Y.P., Wang, C.Z., Chen, W., Zhang, Y.C., Zhang, J., “Research on AC Electronic Load Based on back to back Singlephase PWM Rectifiers,” Applied Power Electronics Conference and Exposition, 2008. APEC 2008. Twenty-Third Annual IEEE. 2008, pp.630-634. 2008. [3] M. Karimi-Ghartimani, S.A. Khajehoddin, P. Jain, A. Bakhshai, “A systematic approach to dc-bus control design in single phase grid connected renewable converters,” IEEE Trans. Power Electron, vol. 28, no. 7, pp. 3158–3166, July. 2013. [4] X. Yuan, F. Wang, D. Boroyevich, Y. Li, and R. Burgos, “Dc-link voltage control of a full power converter for wind generator operating inweak-grid systems,” IEEE Trans. Power Electron., vol. 24, no. 9, pp. 2178–2192, Sep. 2009. [5] S. B. Kjaer, J. K. Pedersen, and F. Blaabjerg, “A review of single-phase grid-connected inverters for photovoltaic modules,” IEEE Trans. Ind. Appl., vol. 41, no. 5, pp. 1292–1306, Sep. 2005. [6] K. G. Pavlou, M. Vasiladiotis, and S. N. Manias, “Constrained model predictive control strategy for single-phase switch-mode rectifiers,” IET. Power Electron., vol. 5, no. 1, pp. 31–40, Dec. 2011. [7] A. Youssef, S. El Khil, and I. Slama-Belkhodja, “State observer-based sensor fault detection and isolation, and fault tolerant control of a single phase PWM rectifier for electric railway traction,” IEEE Trans. Power Electron., vol. 28, no. 12, pp. 5842–5853, Dec. 2013. [8] C.-S. Lam, W.-H. Choi, M.-C. Wong, and Y.-D. Han, “Adaptive dclink voltage-controlled hybrid active power filters for reactive power compensation,” IEEE Trans. Power Electron., vol. 27, no. 4, pp. 1758– 1772, Apr. 2012. [9] A.Bhattacharya and C. Chakraborty, “A shunt active power filter with enhanced performance using ANN-based predictive and adaptive controllers,” IEEE Trans. Ind. Electron., vol. 58, no. 2, pp. 421–428, Feb. 2011.

**AUTHOR'S PROFILE:**

**[1]. M.V.V. SURESH** Pursuing his Masters Degree in Department of EEE from Kakinada Institute Of Technological Sciences (Kits), Ramachandrapuram.

****

**[2]. DANDANGI RAMESH BABU ,** Completed his B.Tech Degree from Aditya Engineering College, Surampalem, Completed his M.Tech Degree from KITS Ramachandrapuram in EEE Department. Presently he is working as Assistant Professor in KITS Ramachandrapuram.. His Interested Area is Power Electronics.