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32-BIT SUPERCONDUCTOR 4×4 BIT-SLICE INTEGER MATRIX MULTIPLIER

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ABSTRACT:

Rapid single-flux-quantum (RSFQ) circuits are expected to be a future integrated circuits technology for its high speed and low power consumption. An 8-bit serial Microprocessor (FLUX-1), bit-serial microprocessors (CORE1 series), a bit-serial asynchronous microprocessor (SCRAM2) , and an 8-bit serial microprocessor (CORE e4) have been designed respectively. A 32-bit 4×4 bit-slice RSFQ matrix multiplier is pro-posed. The multiplier mainly consists of bit-slice multipliers and bit-slice adders. The multiplication of unsigned integer matrixes is implemented by control signals. The matrix multiplier used synchronous concurrent-flow clocking. The results show that 16-bit bit-slice processing has the least latency at 10 GHz.

1. INTRODUCTION

Superconductive physical science is an important key technology, which may support a large selection of fields, like energy, physical science, transportation, drugs and environmental improvement. Superconductor technology allows the belief of apparatus that was unrealizable with typical technology and bears nice anticipation as a technology that can sustain society within the twenty one st century. The distinctive physical properties of superconductive materials and also the connected electrical and magnetic effects area unit applied in many alternative analysis domains. Europe already expressed to launch intergovernmental organizations regarding special society wants and analysis demands . Today, Japan, the U.S.A and Europe area unit smartly competitive within the field of R& amp;D for advanced superconductor technology. The U.S.A. and Japan area unit already in operation national analysis centres for superconductive technology. Building upon our analysis accomplishments inside the FLUXONICS network and by the European cooperation between universities, analysis institutes and industries, we are going to more promote R&D that may cause early applications of digital superconductor devices. within the field of low-integrated analog superconductor devices (e.g. field of force sensors) Europe keeps up with the competitors. However, the overall tendency for analog and digital circuits is to extend the quality significantly. this transformation towards VLSI circuits wants adequate resources and should be addressed during a focussed manner as is completed in U.S.A. and Japan. a eu Superconductive physical

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science Centre (ESEC) will coordinate multidisciplinary programs for analysis, development, and technology transfer within the space of superconductive physical science. the main focus are the effective collaboration between national analysis institutes, universities and trade to determine a replacement physical science family supported quantum effects in superconductors. The speedy Single Flux Quantum (RSFQ) physical science provides Associate in Nursing ultra-low power consumption of solely 1aJ (10.000 times but a contemporary transistor) per operation and is thus a promising future various to today's CMOS physical science. RSFQ is capable to control at clock frequencies higher than a hundred gigahertz. The more growing packaging density in typical integrated CMOS circuits is already restricted by their power density generating an enormous thermal heating.

2. LITERATURE SURVEY

O. A. Mukhanov, S. V. Rylov, V. K. Semenov, and S. V. Vyshenskii, are proposed Several ways to achieve local timing of Josephson-junction RSFQ (rapid single flux quantum) logic elements are proposed. Several examples of serial and parallel pipelined arithmetic blocks using various types of timing are suggested and their possible performance is discussed. Serial devices enable one to perform n-bit functions relatively slowly but using integrated circuits of a moderate integration scale, while parallel pipelined devices are more hardware-wasteful but promise extremely high productivity. The possible local and self-timing of RSFQ logic elements has been demonstrated, making it possible to construct digital blocks and complex devices operating at extremely high clock frequencies, limited only by logic delays of the RSFQ elements (~100 GHz for the present-day Nb technologies).

Q. P. Herr, N. Vukovic, C. A. Mancini, K. Gaj are proposed have designed and RSFQ multiplier-accumulator, the central component of our decimation digital filter. The circuit consists of 38 synchronous RSFQ cells of six types arranged into a rectangular systolic array fed by one parallel input and one serial input. Timing is based on counter-flow clock distribution scheme with simulated maximum clock frequency of 11 GHz. The circuit, fabricated at Hypres, Inc., contains 1100 Josephson junctions, has power consumption less than 0.2 mW, and area less than 2.5 mm/sup 2/. The multiplier-accumulator has been tested at low frequency demonstrating full functionality and stable operation over a 24 hour testing period. This four-bit multiplier accumulator is one of the largest reported RSFQ circuits verified experimentally to date.

Y. Horima, T. Onomi, M. Kobori, are proposed For the improvement of the phase-mode parallel multiplier, we propose to use a Booth encoder as a substitute of an AND array. Booth's algorithm is often used for the generation of partial products. The scale of the encoder does not matter for defining its operation frequency because the phase-mode Booth encoder is a pipelined structure. We suggest that the encoder is used as a serial encoder to reduce the number of Josephson junctions (JJ). There are two methods for

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applying the Booth encoder to the current structure. The first method is shifting multiplicands. The second method is shifting partial products and complementary signals. The total JJ's in both methods are less than the AND array in large scale. The phase-mode Booth encoder with 2.5 kA/cm^2 Nb/AlO$_x$/Nb junctions can operate over 30 GHz according to the numerical simulations.

3.EXISTING SYSTEM:

Rapid single-flux-quantum (RSFQ) circuits are expected to be a future integrated circuits technology for its high speed and low power consumption. An 8-bit serial microprocessor (FLUX-1), bit-serial microprocessors (CORE1 series), a bit-serial asynchronous microprocessor (SCRAM2) , and an 8-bit serial microprocessor (CORE e4) have been designed respectively. And a prototype of a 32-bit superconducting micro-processor based on 4-bit bit-slice architecture has been presented at ASC 2016. Bit-serial processing involves greater latency in processing 32-bit data, while parallel processing will lead to high hardware cost. Therefore we proposed the bit-slice processing which achieves higher speed than bit-serial processing and less hardware cost than parallel processin

4.PROPOSED SYSTEM

The matrix multiplier produces the result of $C=AB$. A, B and C are 4×4 matrixes. Each of the 32-bit elements in A and B is divided into 4 slices of 8 bits each. The four pairs are in-put one by one from the least significant one. The multiplier performs unsigned integer matrix multiplication. Each of the 64-bit elements in C is divided into eight 8-bit slices which are output one by one from the least significant one.

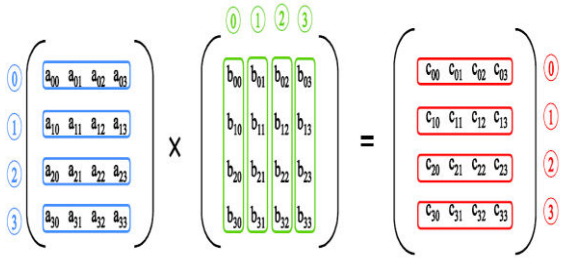

Fig. 1 The diagram of an 8-bit bit-slice 4×4 matrix multiplication.

Fig. 1 shows a diagram of a 4×4 matrix multiplication. The matrix A and B are divided into four rows and four col-umns using four blue and green rectangles, respectively. The matrix product C is divided into four rows using four red rec-tangles.

An 8-bit bit-slice 4×4 matrix multiplication is carried out through 131 steps. (We use 'step' in order to explain the pro-posed matrix multiplication algorithm. It is different from the clock cycle appearing later.) Fig. 2 shows a block diagram of the proposed 8-bit bit-slice 4×4 matrix multiplier. It consists of four 8-bit bit-slice multipliers and three 8-bit bit-slice adders.

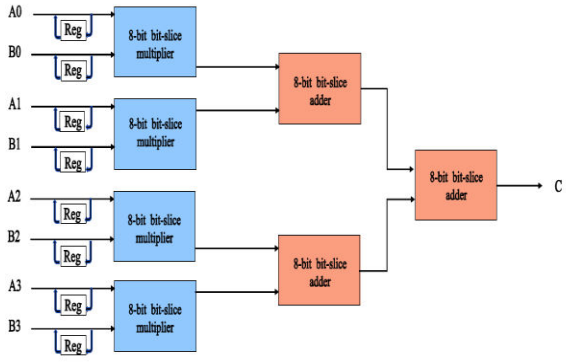

Fig. 2 The block diagram of an 8-bit bit-slice 4×4 matrix multiplier.

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At steps 1 to 11, the *i*-th (*i*=1 to 4) pair of the 32-bit ele-ments in *A* and *B* matrixes is input to the matrix multiplier at *i*-th step. The *i*-th slice of *a*00, *a*01, *a*02 and *a*03 in *A* matrix is fed to input ports *A*0, *A*1, *A*2 and *A*3 at the *i*-th step and fed back to the succeeding 8-bit bit-slice multiplier with 4-step delay. The *i*-th slice of *b*00, *b*10, *b*20, and *b*30 in *B* matrix is fed to input ports *B*0, *B*1, *B*2 and *B*3 at the *i*-th step and fed back to the succeeding 8-bit bit-slice multiplier with 16-step delay. The four 8-bit bit-slice multipliers calculate the products of the *j*-th (*j*=1 to 8) slices of *a*00*b*00, *a*01*b*10, *a*02*b*20, and *a*03*b*30, re-spectively. The two succeeding 8-bit bit-slice adders calculate the sums of the *j*-th slices of *a*00*b*00+*a*01*b*10 and *a*02*b*20+*a*03*b*30, respectively. The last 8-bit bit-slice adder calculates the *j*-th slice of *c*00 at steps 4 to 11.

At steps 9 to 19, the *i*-th slice of *b*01, *b*11, *b*21, and *b*31 in *B* matrix is fed to input ports *B*0, *B*1, *B*2, and *B*3 at the (*i*+8)-th step and fed back to the succeeding 8-bit bit-slice multiplier with 16-step delay. The four 8-bit bit-slice multipliers calcu-late the products of the *j*-th (*j*=1 to 8) slices of *a*00*b*01, *a*01*b*11, *a*02*b*21, and *a*03*b*31, respectively. The two succeeding 8-bit bit-slice adders calculate the sums of the *j*-th slices of *a00b01+a01b11* and *a02b21+a03b31,* respectively. The last 8-bit bit-slice adder calculates the *j*-th slice of *c*01 at steps 12 to 19.

At steps 17 to 27, the *i*-th slice of *b02, b12, b22,* and *b32* in *B* matrix is fed to input ports *B*0, *B*1, *B*2, and *B*3 at the (*i*+16)-th step and fed back to the succeeding 8-bit bit-slice multiplier with 16-step delay. The four 8-bit bit-slice multipliers calcu-late the products of the *j*-th (*j*=1 to 8) slices of *a00b02, a01b12, a02b22,* and *a03b32,* respectively. The two succeeding 8-bit bit-slice adders calculate the sums of the *j*-th slices of *a00b02+a01b12* and *a02b22+a03b32,* respectively. The last 8-bit bit-slice adder calculates the *j*-th slice of *c*02 at steps 20 to 27.

At steps 25 to 35, the *i*-th slice of *b03, b13, b23,* and *b33* in *B* matrix is fed to input ports *B*0, *B*1, *B*2, and *B*3 at the (*i*+24)-th step and fed back to the succeeding 8-bit bit-slice multiplier with 16-step delay. The four 8-bit bit-slice multipliers calcu-late the products of the *j*-th (*j*=1 to 8) slices of *a00b03, a01b13, a02b23,* and *a03b33,* respectively. The two succeeding 8-bit bit-slice adders calculate the sums of the *j*-th slices of *a00b03+a01b13* and *a02b23+a03b33,* respectively. The last 8-bit bit-slice adder calculates the *j*-th slice of *c*03 at steps 28 to 35.

Similarly, the *i*-th slice of *a*10, *a*11, *a*12, and *a*13 in *A* matrix is fed to input ports *A*0, *A*1, *A*2, and *A*3 at the (*i*+32)-th step and fed back to the succeeding 8-bit bit-slice multiplier with 4- step delay. The eight slices of *c*10, *c*11, *c*12, and *c*13 are calcu-lated from steps 33 to 67. The *i*-th slice of *a*20, *a*21, *a*22, and *a*23 in *A* matrix is fed to input ports *A*0, *A*1, *A*2, and *A*3 at the (*i*+64)-th step and fed back to the succeeding 8-bit bit-slice multiplier with 4-step delay. The eight slices of *c*20, *c*21, *c*22, and *c*23 are calculated from steps 65 to 99. The *i*-th slice of *a*30, *a*31, *a*32, and *a*33 in *A* matrix is fed to input ports *A*0, *A*1, *A*2, and *A*3 at the (*i*+96)-th step. The eight

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slices of *c*30, *c*31, *c*32, and *c*33 are calculated from steps 97 to 131.

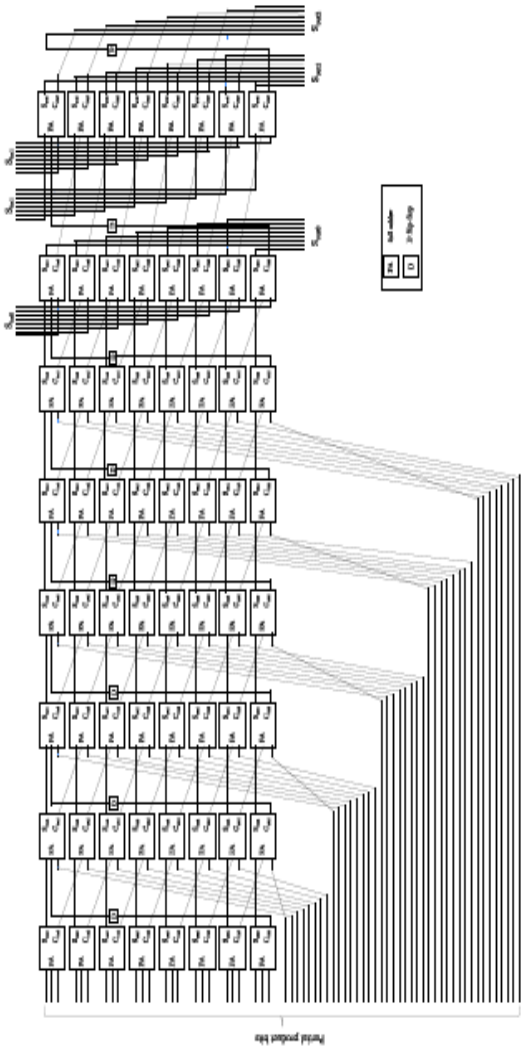

Fig. 3 A block diagram of an 8-8 accumulator.

B. RSFQ Logic Design

We use concurrent flow clocking to design fully pipelined synchronous RSFQ logic circuits of the proposed matrix mul-tiplier. As shown in Fig.2, It consists of four 8-bit bit-slice multipliers and three 8-bit bit-slice adders. And each register (Reg) for holding a slice of *A0-A3* is implemented using four D flip-flops (DFFs). Each Reg for holding a slice of *B0-B3* is implemented using sixteen DFFs. An 8-bit bit-slice multiplier is designed using the approach as in [15]. Fig. 3 shows a block diagram of an 8-8 accumulator which is a part of 8-bit bit-slice multiplier. In the figure, the upper side is the LSB si-de and the lower side is the MSB side. The 8-8 accumulator consists of eight 8-bit carry save adders each of which is a row of eight full adders. The DFFs are required to keep the carries from the most significant position of the correspond-ing slices and add them to the least significant position of the succeeding slices. Each full adder is implemented using two AND gates, two XOR gates, two DFFs, and a CB. An 8-bit bit-slice integer multiplier contains the four main blocks.

PARAMETER	**EXISTING METHOD**	**PROPOSED METHOD**
DELAY	24.846ns	15.467ns
AREA	2213LUT's	7600LUT's
POWER	3.666	3.645

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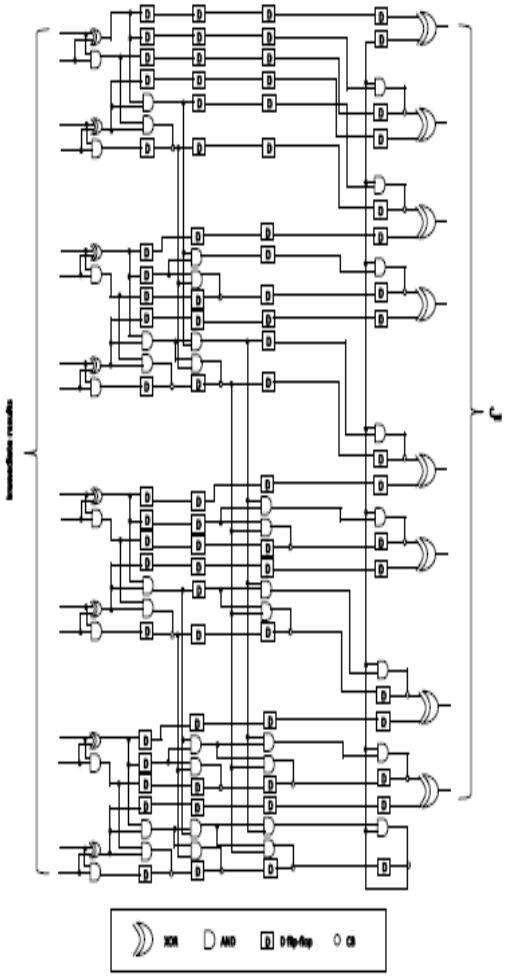

Fig. 4 A logic level circuit of 8-bit bit-slice adder.

Fig. 4 shows an RSFQ logic design of the 8-bit bit-slice adder. We use a type of parallel prefix adder called Sklansky adder to implement it. The block consists of 6 pipeline stages. The delay in the feedback loop for the carry signal to the suc-ceeding slice is minimized using the technique developed in Four pairs of each element slices in the first row of ma-trix *A* and in the first column of matrix *B* are fed at the first to forth clock cycles. The four slices of each element in the first row of matrix *A* are held for four clock cycles and the four slices of each element in the first column of matrix *B* are held for sixteen clock cycles. The four slices of each element in the second column of matrix *B* are fed at the fifth to eighth clock cycles, and so on. Eight slices of each row element in matrix produce *C* are output at the 48th to 175th clock cycles.

5. RESULTS ANALYSIS

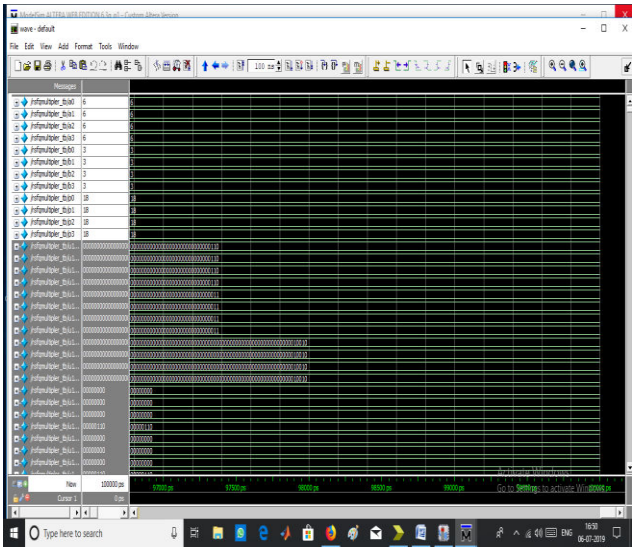

Fig 5 Simulation Result

Table.1 Comparison Table

Table 1 shows the power and delay comparison of the proposed multiplier with other multiplier designs. It is also shown from the table that the proposed designed is better in terms of power and delay.

6. CONCLUSION

The use of a basic set of RSFQ elementary cells based on flip-flops rather than on combinational gates leads to the development of efficient and compact DSP functions of mUltiply, add, and accumulate. Flow timing of RSFQ circuits has proven to be practical in the implementation of relatively large DSP circuits. The choice of concrete flow-timing scheme depends on the

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applications. The proper choice of a timing scheme leads to maximization of operating speed and to reducing of the layout burden of extra JTLs used for clock distribution. Unambiguous RSFQ circuit testing at frequencies above 2 GHz has been demonstrated using an on-chip shift register-based test system. This system enables circuit test at full GHz speeds while communicating with semiconductor electronics at low speed. Finally, we have designed, fabricated, and evaluated at high-speed an RSFQ library of multiply-add-accumulate elements with high throughput suitable for the implementation of a variety of DSP processors. To our knowledge, our 6.3 GHz serial multiplier and 13.7 GHz module of parallel multiplier are the fastest DSP circuits to date.

REFERENCES

[1] O. A. Mukhanov, S. V. Rylov, V. K. Semenov, and S. V. Vyshenskii, "RSFQ logic arithmetic," IEEE Trans. Magn., vol. 25, no. 2, pp. 857–860, Mar. 1989.

[2] O. A. Mukhanov and A. F. Kirichenko, "Implementation of a FFT radix 2 butterfly using serial RSFQ multiplier-adders," IEEE Trans. Appl. Supercond., vol. 5, pp. 2461–2464, Jun. 1995.

[3] S. V. Polonsky, J. C. Lin, and A. V. Rylyakov, "RSFQ arithmetic blocks for DSP applications," IEEE Trans. Appl. Supercond., vol. 5, pp. 2823– 2826, Jun. 1995.

[4] Q. P. Herr, N. Vukovic, C. A. Mancini, K. Gaj, K. Qing, V. Adler, E. G. Friedman, A. Krasniewski, M. F. Bocko, and M. J. Feldman, "Design and low speed testing of a four-bit RSFQ multiplier-accumulator," IEEE Trans. Appl. Supercond., vol. 7, no. 2, pp. 3168–3171, Jun. 1997.

[5] A. Akahori, M. Tanaka, A. Sekiya, A. Fujimaki, and H. Hayakawa, "Design and demonstration of SFQ pipelined multiplier," IEEE Trans. Appl. Supercond., vol. 13, no. 2, pp. 559–562, Jun. 2003.

[6] M. Obata, M. Tanaka, Y. Tashiro, Y. Kamiya, N. Irie, K. Takagi, N. Takagi, A. Fujimaki, N. Yoshikawa, H. Terai, and S. Yorozu, "Singleflux- quantum integer multiplier with systolic array structure," Phys. C, vol. 445–448, pp. 1014–1019, 2006.

[7] I. Kataeva, H. Engseth, and A. Kidiyarova-Shevchenko, "New design of an RSFQ parallel multiply accumulate unit," Supercond. Sci. Technol., vol. 19, pp. 381–387, May 2006.

[8] Y. Horima, T. Onomi, M. Kobori, I. Shimizu, and K. Nakajima, "Improved design for parallel multiplier based on phase-mode logic," IEEE Trans. Appl. Supercond., vol. 13, no. 2, pp. 527–530, Jun. 2003.

[9] R. Nakamoto, S. Sakuraba, T. Onomi, S. Sato, and K. Nakajima, "4-bit SFQ multiplier based on Booth encoder," IEEE Trans. Appl. Supercond., vol. 21, no. 3, pp. 852–855, Jun. 2011.

[10] S. Yorozu, Y. Kameda, H. Terai, A. Fujimaki, T. Yamada, and S. Tahara, "A single flux quantum standard logic cell library," Phys. C, vol. 378, pp. 1471–1474, 2002.

[11] H. Hara, K. Obata, H. Park, Y. Yamanashi, K. Taketomi, N. Yoshikawa, M. Tanaka, A. Fujimaki, N. Takagi, K. Takagi, and S. Nagasawa, "Design, implementation

2581-4575
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Crossref
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and on-chip high-speed test of SFQ half-precision floating-point multiplier," IEEE Trans. Appl. Supercond., vol. 19, pt. 1, no. 3, pp. 657–660, Jun. 2009.

[12] J. L. Hennessy and D. A. Patterson, Computer Architecture: A Quantitative Approach, 5th ed. Elsevier, 2012.